DESIGN AND ANALYSIS OF VLSI SUBSYSTEMS

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PRE-REQUISITES : Digital Electronics at Undergraduate level.

INTENDED AUDIENCE : Students interested in Digital VLSI

INDUSTRIES APPLICABLE TO : Samsung, Intel, Broadcom, Qualcomm, IBM

COURSE OUTLINE :

The course will introduce students to the topics of Digital CMOS VLSI subsystem design using design metrics of delay, power, and area in detail. The course focuses more on power estimation, and interconnect aware designs and discusses on few power benefits designs. Approximate computing datapath subsystem designs will be analyzed along with the design, and error metrics. Different forms of standard cell design of latch, and flipflops will be discussed and the importance of timing parameters in sequential circuits will explained.

ABOUT INSTRUCTOR :

Prof.Madhav Rao is an Associate Professor at IIIT-Bangalore. He teaches Digital VLSI Design, VLSI subsystem, Electronic devices and circuits, and basic electronics courses to IIIT-B students. He is a recipient of SERB Early Career Research Award (2014-2017), Visvesvaraya Young Faculty fellowship award (2016-2020), IBM Shared University Research Award (2018-20), 2021 IBM Global University Program Academic Award. He has also completed projects sponsored by MEITY in the past, and is currently involved in the project from MSJE, and GoK, IT-BT center.

COURSE PLAN :

Week 1**:** CMOS Transistors and Current model

Week 2**:** CMOS Inverter and characteristics

Week 3**:** Noise Margin and Delay of Inverter

Week 4**:** RC Delay

Week 5**:** Delay optimization

Week 6**:** Combinatorial Circuit Family

Week 7**:** Stick Diagram & Interconnects

Week 8**:** Interconnects (Contd)

Week 9**:** Power

Week 10**:** Static Power, and CMOS Latch and flipflop design

Week 11**:** Static Timing Analysis

Week 12**:** Adder subsystem design, and Approximate Computing