Advanced Logic Synthesis - Video course

COURSE OUTLINE

- The goal of the course is to study the components of digital design & advanced concepts in synthesis process
- To understand the importance of technology, libraries, design constraints, design rules
- To understand the usefulness of reports with respect to design on Area, Timing & Power
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Learning Outcomes:

- Ability to set constraints, Validate the results and analyze the reports
- Ability to synthesize the design based on Area and Timing priority
- Ability to perform critical path synthesis
- Ability to perform timing analysis on the synthesized netlist
- Ability to verify the functional equivalence of the synthesized netlist Vs RTL

COURSE DETAIL

Unit No	Title
1	**MOS Transistor** M o s Transistor, Logic, Pmos Transistor, Nmos Transistor, CMOS Transistor, Design of basic gates, combinational circuits and sequential circuits using MOS transistor logic. Stick diagrams and layout diagrams for basic circuits, Lambda Based Rules, Calculation of propagation delays

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Electronics & Communication Engineering

Coordinators:

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2	**Digital timing in CMOS** Static CMOS circuit, NMOS Transistors in Series/Parallel Connection, PMOS Transistors in Series/Parallel Connection, Complex CMOS Gate, Cell Design, Standard Cells, Stick Diagrams, Switch Delay Model, Fast Complex Gates, Sizing Logic Paths for Speed, Logical Effort of Gates, Multistage Networks, Ratioed Logic, Pseudo-NMOS Sequential logic, Latch versus register, Latch-Based Design, Maximum Clock Frequency, Meta-Stability, Mux-Based Latches, Master-Slave (Edge-Triggered) Register, Setup/Hold Times Wire Load Model. Linear timing model. Non linear delay model (NLDM). Timing models for combinational & sequencial cells. Clock specification, Basic clock specification. Extended clock specification. Clock uncertainty. Inter-clock uncertainty. Master clock latency. Generated clocks. Divided clock. Multiplied clock. Gated clock. Master clock at clock gating cell output. Edge_shift option. Generated clock latency. .	
3	**Process Of Synthesis, Libraries And Technology Mapping** Introduction to synthesis, synthesizable and non synthesizable constructs. Logical synthesis of basic combinational and sequential circuits.Synthesis Methodologies. Pre and post synthesis mismatch. Translation, mapping and optimization. Overview of Libraries: Target library, synthetic library, symbol library and link Library. Reading the design. Design constraints: design rule constraints and optimization constraints. Optimization for power, timing and area. Compile strategies in synthesis. Design analysis. Importance of wire load models. Specifying operating conditions and system interface characteristics	
4	**Advanced Synthesis flow** Post synthesis flow and analysis. Advanced critical path resynthesis, grouping and ungrouping the designs, cost priorities, optimization with timing and area efforts. Register retiming. Incremental, power and dft flows in synthesis	

5	**Timing Analysis** Introduction to timing concepts. Setup and hold times. Setup and hold time equalities and inequalities. Timing paths. Static timing delay calculation for basic flip flop & sequential circuits. Definition of “timing path”. Grouped timing paths. Timing path delay. Recovery and removal times. Pulse width, signal slew. Clock latency. Clock skew. Input arrival time. Output required time. Slack and critical path. False paths. Multi-cycle paths.

References:

- Instructor reference material
- Digital Design by M. Morris Mano, 4th edition, PHI Publishers
- Tool user guides
- Fundamentals of digital circuits by A.Anand Kumar, 2nd Edition, PHI Publishers