

# VLSI Circuits - Video course

## 1 Introduction to VLSI Design

Introduction

## 2 Combinational Circuit Design

Components of Combinational Design - Multiplexer and Decoder

Multiplexer Based Design of Combinational Circuits

Implementation of Full Adder using Multiplexer

Decoder

Implementation of Full Adder using Decoder

## 3 Programmable Logic Devices

Types of Programmable Logic Devices

Combinational Logic Examples

PROM - Fixed AND Array and Programmable OR Array

Implementation of Functions using PROM

PLA - Programmable Logic Array

PLA - Implementation Example

## 4 Programmable Array Logic

PAL - Programmable Array Logic

Comparison of PROM, PLA and PAL

Implementation of a Function using PAL

Types of PAL Outputs

Device Examples

## 5 Review of Flip-Flops

Introduction to Sequential Circuits

R-S Latch and Clocked R-S Latch

D Flip Flop

J-K Flip Flop

Master Slave Operation

Edge Triggered Operation

## 6 Sequential Circuits

Clocking of Flip-flops

Setup and Hold Times

Moore Circuit

Mealy Circuit

Clocking Rules

Sequential Circuits - Design Rules

## 7 Sequential Circuit Design

Sequential Circuit Design Basics

Design of a 4-bit Full Adder using D Flip-flop

Pattern Identifier

State Graph

Transition Table

## 8 MSI Implementation of Sequential Circuits

Implementation of Pattern Identifier revisited

MUX Based Realization

ROM Based Realization

PAL Implementation

## 9 Design of Sequential Circuits using One Hot Controller

Design of a Vending Machine as an example

State Graph

State Table

Implementation using PAL

## 10 Verilog Modeling of Combinational Circuits

Introduction to Verilog

Levels of Abstraction

Realization of Combinational Circuits

Verilog Code for Multiplexers and Demultiplexers

Realization of a Full Adder

Behavioral, Data Flow and Structural Realization

Realization of a Magnitude Comparator

Design Example

## 11 Modeling of Verilog Sequential Circuits - Core Statements

Design of a D Flip Flop

Realization of a Register

Realization of a Counter

Realization of a Non-retriggerable Monoshot

## 12 Modeling of Verilog Sequential Circuits - Core Statements (Continued)

Realization of a Right Shift Register

Realization of a Parallel to Serial Converter

Realization of a Model State Machine

Pattern Sequence Detector as a Design Example

## 13 RTL Coding Guidelines



NP-TEL

# NPTEL

<http://nptel.ac.in>

## Electronics & Communication Engineering

**Coordinators:**

**Prof. S. Srinivasan**

Department of Electrical Engineering IIT Madras

RTL Coding Guidelines – Introduction  
Dos and Don'ts for Asynchronous and Synchronous Logic Circuit Design  
RTL Coding Style  
Separation of Combinational and Sequential Circuits  
“if - else if – else” statements for MUX and Priority Encoder Realizations  
Verilog Directives – Case Statements  
Operators

#### **14 Coding Organization - Complete Realization**

Introduction to Coding Organization  
Design Module – a Model  
Complete Code for Combinational and Sequential Circuits

#### **15 Coding Organization - Complete Realization (Continued)**

Complete Code for Sequential Circuits

- Right Shift Register
- Parallel to Serial Converter
- Model State Machine
- Pattern Sequence Detector

Test Bench for Combinational Circuits

#### **16 Writing a Test Bench**

Test bench for simple design – AND gate  
Test bench for Combinational Circuits  
Test bench for Sequential Circuits

#### **17 System Design using ASM Chart**

Top-down Design Methodology

ASM Chart

Rules of Drawing ASM Chart

#### **18 Example of System Design using ASM Chart**

Design of Bus Arbiter

ASM Chart

State Table

Implementation of Bus Arbiter using MUX and D Flip-flops

Specification of a Traffic Light Controller

State Graph

ASM Chart of Traffic Light Controlle

#### **19 Examples of System Design using Sequential Circuits**

Algorithm of Traffic Light Controller

ASM Table

Hardware Realization using MUX and D Flip-flops

Traffic Light Controller – ROM Realization - ROM Table

#### **20 Examples of System Design using Sequential Circuits (Continued)**

Dice Game - Introduction

Algorithm for Dice Game

Architecture

ASM Chart for Dice Game

#### **21 Microprogrammed Design**

Introduction to Microprogrammed Design of Digital Systems

ASM Chart for a Microprogrammed Design

Microprogrammed ROM Table

Comparison of the Conventional ROM and the Microprogrammed ROM Approaches

Single Qualifier, Double address Design

#### **22 Microprogrammed Design (Continued)**

Single Qualifier, Single Address (SQSA) System Design

ASM chart for SQSA Microprogrammed Implementation

Microprogrammed Table

Implementation of SQSA System using Microprogrammed ROM, MUX and a Counter

Dice Game using Microprogrammed SQSA System

ASM Chart and Microprogrammed Table for Dice game

#### **23 Design Flow of VLSI Circuits**

Top-down Design Methodology

Bottom-up Design Methodology

Simulation of Verilog Codes using Modelsim

Test Bench and Simulation of a Simple Design

#### **24 Simulation of Combinational Circuits**

Simulation of Combinational Circuits

Simulation Waveforms

- Simple Gates
- Simple Boolean Expressions
- Shift Register
- MUX and DEMUX

#### **25 Simulation of Combinational and Sequential Circuits**

Simulation Waveforms

- a Magnitude Comparator
- a Design Example
- a D Flip-flop
- Registers
- a Counter

#### **26 Analysis of Waveforms using Modelsim**

Analysis of Waveforms

- a Counter
- a Non-retriggerable Monoshot
- a Right Shift Register
- a Parallel to Serial Converter

- a Model State Machine

### **27 Analysis of Waveforms using Modelsim (Continued)**

Analysis of Waveforms of a Model State Machine (Continued)

Analysis of Waveforms of a Pattern Sequence Detector

### **28 ModelSim Simulation Tool**

ModelSim Command Summary

### **29 Synthesis Tool**

More Features of Modelsim

Synplify Synthesis Tool

Features of Synplify Tool

### **30 Synthesis Tool (Continued)**

Synthesis Tool – Command Summary

Analysis of Design Example using Synplify Tool

### **31 Synplify Tool - Schematic Circuit Diagram View**

Analysis of the Report File generated by Synplify Tool

Commands Continued – Optimized Verilog File using Synplify Tool

Viewing Verilog Code as RTL Schematic Circuit Diagrams

### **32 Technology View using Synplify Tool**

Technology View using Synplify Tool

Warnings and Errors – Log Report

Comparison of FPGA Performance of different Vendors for a Design

Creation of Errors Deliberately and Correction using Modelsim and Synplify Tools

### **33 Synopsys Full and Parallel Cases**

Compilation/Load Errors and Correction using Modelsim and Synplify Tools (Continued)

Synopsys Full Case - RTL View

Synopsys Parallel Case - RTL View

Xilinx Place & Route Tool – Design Manager

Xilinx Place & Route Tool – Command Summary

Place & Route Tool Report

### **34 Xilinx Place & Route Tool**

Xilinx Place & Route Tool Report

Creation of “Bit” File

Synthesis Revisited – Waveform Analysis of Optimized File

Various Report Files of Xilinx Place & Route Tool

Back Annotation in DOS Mode using Xilinx Place & Route Commands

### **35 Xilinx Place & Route Tool (Continued)**

Back Annotation in DOS Mode using Xilinx Place & Route Commands (Continued)

Simulation of Back Annotated File using Modelsim Tool

Analysis of Back Annotated Waveforms to get the Gate Delays of a Design

User Constraint File

Xilinx Floor Planner

Design of PCI Arbiter using ASM Chart - Introduction

### **36 PCI Arbiter Design using ASM Chart**

Design of PCI Arbiter (Continued)

ASM Chart

Verilog Code of PCI Arbiter

Test Bench for the PCI Arbiter Design

Simulation Results after Back annotation

Synplify Results

Xilinx Place and Route Results

### **37 Design of Memories - ROM**

On-chip Dual Address ROM Design

Test Bench for Dual Address ROM Design

Simulation Results

Synplify and Place & Route Results

On-chip Single Address ROM Design

Test Bench for Single Address ROM Design

Simulation Results

Synplify and Place & Route Results

### **38 Design of Memories - RAM**

Design of On-chip Dual RAM

RTL Verilog Code

Test Bench for Dual RAM Design

Simulation Results

Synplify and Xilinx Place & Route Results

### **39 Design of External RAM**

Controller Design for External RAM

Verilog Code for Controller of External RAM

Test Bench for External RAM – GO-No GO Test

Simulation Waveform

Synplify and Xilinx Place & Route Results

### **40 Design of Arithmetic Circuits**

Principle of Pipelining

Partitioning of a Design

Serial Signed Adder Design

Synplify and Xilinx Place & Route Results

Test Bench for Serial Adder

Comparison of a Serial Adder and a Parallel Adder Implementation

Simulation Waveform

### **41 Design of Arithmetic Circuits (Continued)**

Design of Eight Inputs Signed Parallel Adder  
Design Partition

Verilog Code for the Signed Parallel Adder

Test Bench for Parallel Adder

Simulation Waveform

Synplify and Xilinx Place & Route Results

Parallel, Pipelined Multiplier Design – A new Algorithm for Fast Implementation

Verilog Code for the Parallel, Pipelined Multiplier

#### **42 Design of Arithmetic Circuits (Continued)**

Verilog Code for Parallel Multiplier (Continued)

Test Bench for Parallel Multiplier

Simulation Results of Back Annotated Parallel Multiplier Design

Synplify and Xilinx Place & Route Results

#### **43 System Design Examples**

Verilog Code for Traffic Light Controller

Simulation Results of Traffic Light Controller Design

Synplify and Xilinx Place & Route Results

#### **44 System Design Examples (Continued)**

Test Bench for Traffic Light Controller

Introduction to Image/Video Compression

Block Diagram of a Video Encoder

A Novel, Parallel Algorithm for Fast Evaluation of Discrete Cosine Transform and

Quantization (DCTQ)

#### **45 System Design Examples (Continued)**

Design of Discrete Cosine Transform and Quantization Processor

DCTQ Processor Block Diagram

Signal Description of DCTQ Processor

Architecture of DCTQ Processor

Sequence of Operations of a Host Processor and the DCTQ Processor

Verilog Codes for DCTQ Design

#### **46 System Design Examples (Continued)**

Verilog Codes for DCTQ Design (Continued)

DCTQ Top Design Code

Partial Products Register Code

DCTQ Controller Code

#### **47 System Design Examples (Continued)**

Verilog Code for DCTQ Design - DCTQ Controller Code (Continued)

Test Bench for DCTQ Design

Synplify Results

Xilinx Place and Route Results

Analysis of Waveforms of DCTQ Design

Verification of Verilog DCTQ – IQIDCT Cores

Matlab Codes for Pre-processing and Post-processing of an Image

Results – Original and Reconstructed Image Example

Implementation Results of DCTQ, IQIDCT, DCT and IDCT Cores on FPGA/ASIC

Capabilities of IP Cores

#### **48 System Design Examples using FPGA Board**

Design Applications using FPGA Board

- Traffic Light Controller and Real Time Clock

XSV FPGA Board Features

Testing of FPGA Board

Setting the XSV Board Clock Oscillator Frequency

Downloading Configuration Bit Streams

#### **49 System Design Examples using FPGA Board (Continued)**

Features of Digital Input/Output Card

Typical Push Button Debouncing Circuit and Switch Interface Circuits

Typical Driving Circuit for Seven Segment and Discrete LEDs

Problem on FPGA Boards and its Solution

Hardware Setup for Traffic Light Controller

Demo of Traffic Light Controller

Revised Verilog Code Incorporating Blink Control and Pedestrian Crossing

#### **50 Advanced Features of Xilinx Project Navigator**

User Constraint File for Traffic Light Controller

Place and Route and Back Annotation Using Xilinx Project Navigator

- Command Summary of Navigator

Floor Plan

Simulation of Back Annotated File

#### **51 System Design Examples using FPGA Board (Continued)**

Real Time Clock Design

Features and Specification

Block Diagram and Signal Descriptions of Real Time Clock

Simplified Architecture of Real Time Clock

Verilog RTL Code for Real Time Clock

#### **52 System Design Examples using FPGA Board (Continued)**

Verilog RTL Code for Real Time Clock (Continued)

- Real Time Clock Code

- Stop Watch Code

#### **53 System Design Examples using FPGA Board (Continued)**

Stop Watch Implementation (Continued)

Alarms routine

Display ROM Sub-module

Test Bench for Real Time Clock

**54 System Design Examples using FPGA Board (Continued)**

Test Bench for Real Time Clock Design

User Constraint File for Real Time Clock Design

Synplify Results

Xilinx Place and Route Results

Waveform Analysis of the Real Time Clock Design

Demo of the Real Time Clock

**55 Project Design Suggested for FPGA/ASIC Implementations**

Projects Suggested for FPGA/ASIC Implementations

Issues Involved in Digital VLSI System Design

Detailed Specification for Electrostatic Precipitator Controller

Detailed Specification for JPEG/H.261/MPEG Codec

References

Conclusions