VLSI Data Conversion Circuits - Video course

COURSE OUTLINE

This course covers the analysis and design of CMOS Analog-to-Digital and Digital-to-Analog Converters,with about 7 design assigments. The syllabus is as follows :

(i) Introduction to A/D and D/A conversion : sampling, quantization, quantization noise, aliasing and reconstruction filtering.

(ii) ADC/DAC metrics : Differential and Integral Nonlinearity, SNR, SNDR, SFDR and dynamic range.

(iii) ADC Architectures : Will cover two of these architectures in detail
(a) Flash and Floding ADCs.
(b) Oversampling Converters.
(c) Successive Approximation Converters.

(iv) DAC Design :
(a) Current steering DACs**.**

There will be biweekly design assignments (MATLAB/Cadence).

COURSE DETAIL

Lecture No	Course Title
1	Course overview and introduction.
2	Sampling, Spectral properties of sampled signals, Oversampling and its implications on anti-alias filter design.
3	Time Interleaved Sampling, Analysis of a Ping-Pong Sampling system.

NPTEL

http://nptel.iitm.ac.in

Electronics & Communication Engineering

Pre-requisites:

1. Analog Circuits, Networks and Systems, DSP.

Additional Reading:

1. Understanding Delta-Sigma Data Converters : R.Schreier and G.Temes.
2. John Wiley CMOS Data Converters for Communications : N.Tan, Springer.

Hyperlinks:

1. Papers from IEEExplore http://www.ieeexplore.ieee.org

Coordinators:

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4	Ping-pong Sample and Holds continued, Analysis of Offset and Gain Errors in Time-Interleaved Sample and Holds.
5	Sampling Circuits (NMOS, PMOS and CMOS Switches), Distortion due to the Sampling Switch.
6	Thermal Noise in Sample and Holds, Charge Injection in a Sampling Switch.
7	Bottom Plate Sampling, The Gate Bootstrapped Switch.
8	The Gate Bootstrapped Switch (continued), the Nakagome Charge-Pump.
9	Characterizing a Sample-and-Hold, Correct choice of input frequency, Discrete Fourier Series Refresher.
10	FFT Leakage and the Rectangular Window.
11	FFT Leakage (contd), Spectral Windows, the Hann Window
12	Spectral Windows (contd), the Blackman Window, Introduction to Switch Capacitor Amplifiers
13	Switch Capacitor Circuits, Parasitic Insensitive SC Amplifiers
14	Nonidealities in SC Amplifiers - Finite Opamp Gain and DC Offset., Lecture 14 - Part 2 - Finite Opamp Gain-Bandwidth Product.
15	Introduction to Fully Differential Operation.

16	Fully-differential operation (contd), motivation for common-mode feedback.
17	Fully Differential SC-circuits, the "Flip-Around" Sample and Hold, DC Negative Feedback in SC Circuits.
18	ADC Terminology, Offset and Gain Error, Differential Nonlinearity (DNL).
19	Integral Nonlinearity (INL), Dynamic Characterization of ADCs, SQNR, Quantization Noise Spectrum.
20	Quantization Noise Spectrum (contd), SFDR, Flash A/D Converter Basics.
21	Flash A/D Converter Basics, the Regenerative Latch.
22	The Regenerative Latch (contd).
23	Motivation to use a Preamp, Preamp Offset Correction (Autozeroing).
24	Autozeroing a Differential Preamp, Subtracting References from the Input.
25	Coupling Capacitor Considerations in an Autozeroed Preamp.
26	Transistor Level Preamp Design.
27	Necessity of an up-front sample and hold for good dynamic performance. Timing issues in a flash ADC.

28	Bubble Correction Logic in a Flash ADC, Comparator Metastability, Case Study.(VERY POOR AUDIO QUALITY !)
29	Flash ADC Case Study (Continued).
30	D/A Converter Basics, INL/DNL, DAC Spectra and Pulse Shapes.
31	NRZ vs RZ DACs, DAC Architectures.
32	Binary Weighted versus Thermometer DACs.
33	Binary vs Thermometer DACs (Contd), Current Steering DACs.
34	Current Steering DACs (contd) .
35	Current Cell Design in a Current Steering DAC.
36	Current Cell Design (contd), Layout Considerations in Current Steering DACs.
37	Oversampled Approaches to Data Convresion, Benefits of Oversampling.
38	Oversampling with Noise Shaping, Signal and Noise Transfer Functions, First and Second Order Delta-Sigma Converters.
39	Signal Dependent Stability of DSMs, the Describing Function Method.
40	Stability in DSMs (continued).
41	Maximum Stable Amplitude of DSMs and

	Relation to Out of Band Gain, Systematic NTF Design.
42	Systematic NTF Design (contd), the Bode Sensitivity Integral and its Implications on NTF Design.
43	Estimating the Maximum Stable Amplitude from simulation, Computation of in-band SNR, Windowing revisited.
44	Introduction to Continuous-time Delta Sigma Modulators (CTDSM).
45	CTDSM basics (contd), time-scaling of CTDSMs.
46	The inherent anti-aliasing property of CTDSMs.
47	Excess Loop Delay in CTDSMs.
48	Time-constant changes in CTDSMs, Influence of opamp nonidealities.
49	Effect of opamp nonidealities (contd) - finite gain bandwidth, Effect of ADC and DAC nonidealities.
50	Effect of DAC element mismatch (contd), Dynamic Element Matching (Randomization).
51	Dynamic Element Matching by Data Weighted Averaging.
52	Effect of Clock jitter in CTDSMs.
53	Finding Loopfilter Coefficients in Higher

	Order CTDSMs.
54	Dynamic Range Scaling of the Loop Filter.

References:

1. Understanding Delta - Sigma Data Converters: R. Schreier, Wiley.
2. Course handouts.
3. Research papers from the IEEE Journal of Solid State Circuits and the IEEE Transactions on Circuits and Systems.