CMOS DIGITAL VLSI DESIGN

PROF. SUDEB DASGUPTA

Department of Electronics and Communication Engineering

IIT Roorkee

PRE-REQUISITES : A basic course of Semiconductor Devices and Digital Electronics. A course on Computer Organization will be quite helpful.

INTENDED AUDIENCE : Final year Undergraduates and/or First year Master Student (Microelectronics)

INDUSTRIES APPLICABLE TO : Cadence, Synopsys, ST Microelectronics, NXP Semiconductors, SCL, Chandigarh

COURSE OUTLINE :

This course brings circuit and system level views on design on the same platform. The course starts with basic device understanding and then deals with complex digital circuits keeping in mind the current trend in technology. The course follows a design perspective, starts from basic specifications and ends with system level blocks. Eight Assignments are provided which will add/help in understanding the course in a better manner both at conceptual as well as hands-on level.

ABOUT INSTRUCTOR :

Prof. S. Dasgupta,is presently working as an Associate Professor, in Microelectronics and VLSI Group of the Department of Electronics and Communication Engineering at Indian Institute of Technology, Roorkee. He received his PhD degree in Electronics Engineering from Institute of Technology-Banaras Hindu University (currently IIT-BHU), Varanasi in 2000. During his PhD work, he carried out research in the area of effects of ionizing radiation on MOSFET. Subsequently, he was member of faculty of Department of Electronics Engg.,at Indian School of Mines, Dhanbad (currently IIT-Dhanbad). In 2006, he joined as an Assistant Professor in the Department of Electronics and Communication Engineering at Indian Institute of Technology, Roorkee. He is currently the Chairman, Faculty Search Committee of the Department. He has authored/co-authored more than 200 research papers in peer reviewed international journals and conferences. His citations are around 2400 (after 2006) and h-index and i-index are 25 and 65 respectively. He is a member of IEEE, EDS, ISTE and associate member of Institute of Nanotechnology, UK. He has been a technical committee member International Conference on Micro-to-Nano, 2006; VDAT-2012, 13, 14, 15, 16, 17 and 18. He worked as the Organising Chair and Program Co-Chair for VDAT-2017 held at IIT Roorkee. He is also heading the Technical Program Group for Emerging Devices at VLSI Design Conference. He has presented tutorial in VDAT-2014 and VLSI Design Conference, Bangalore 2015 amongst many others. He has also been member of technical committees of various international conferences. He has presented large number of invited and keynote talk at various technical forum. He was awarded with Erasmus Mundus Fellowship of European Union in the year 2010 to work in the area of RDF at Politecnico Di Torino, Italy. He is the recipient of prestigious IUSSTF to work in the area of SRAM testing at University of Wisconsin at Madison, USA in the year 2011-12. He was also awarded with DAAD Fellowship to work on Analog Design using Reconfigurable Logic at TU, Dresden, Germany in the year 2013. He is the Principal Coordinator for SMDP-C2SD at IIT Roorkee. His areas of interest are Nanoelectronics, Nanoscale MOSFET modeling and simulation, Design and Development of low power novel devices, FinFET based Memory Design, Emerging Devices in Analog Design and Design and development of reconfigurable logic. He has guided/co-guided 15Ph.D scholars. Currently he is supervising 7 candidates leading to their Ph.D degree. He has been awarded INAE Young Engineer Award. Dr. Dasgupta acted as a reviewer for IEEE Transactions on Electron Devices, IEEE Electron Device Letters, IEEE Transactions on Nanotechnology, Superlattice and Microstructures, International Journal of Electronics, Semiconductor Science and Technology, Nanotechnology, IEEE Transactions on VLSI Systems, Microelectronic Engineering, and Microelectronic Reliability amongst other.

COURSE PLAN :

Week 1 : MOS Transistor Basic-I; L2: MOS Transistor Basic-I; L3: MOS Transistor Basic-II; L4: MOS Parasitic & SPICE Model; L5: CMOS Inverter Basics-I

Week 2 : CMOS Inverter Basics-II; L2: CMOS Inverter Basics-III; L3: Power Analysis-I; L4: Power Analysis-II; L5: SPICE Simulation-I

Week 3 : SPICE Simulation-II; L2: Combinational Logic Design-I; L3: Combinational Logic Design-II; L4: Combinational Logic Design-III; L5: Combinational Logic Design-IV

Week 4 : Combinational Logic Design-V; L2: Combinational Logic Design-VI; L3: Combinational Logic Design-VII; L4: Combinational Logic Design-VIII; L5: Combinational Logic Design-IX

Week 5 : Combinational Logic Design-X; L2: Logical Efforts-I; L3: Logical Efforts-II; L4: Logical Efforts-III; L5: Sequential Logic Design-I

Week 6 : Sequential Logic Design-II; L2: Sequential Logic Design-III; L3: Sequential Logic Design-IV; L4: Sequential Logic Design-V; L5: Sequential Logic Design-VI

Week 7 : Sequential Logic Design-VII; L2: Sequential Logic Design-VIII; L3: Clocking Strategies for Sequential Design-I; L4: Clocking Strategies for Sequential Design-II; L5: Clocking Strategies for Sequential Design-III

Week 8 : Clocking Strategies for Sequential Design-IV; L2: Sequential Logic Design-IX; L3: Clocking Strategies for Sequential Design-V; L4: Concept of Memory & its Designing-I; L5: Concept of Memory & its Designing-II