ANALOG ELECTRONIC CIRCUITS - IITM

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PRE-REQUISITES : High school mathematics, basic circuit theory

INTENDED AUDIENCE : Undergraduate students, graduate students

INDUSTRY SUPPORT : All semiconductor design / services companies

COURSE OUTLINE :

This course is intended to introduce students to the fascinating world of analog electronics. The emphasis of the course is to build intuition behind the operation of circuits. To do this, we derive circuits ground-up, from first principles. The student is expected to have undergone a basic linear-circuit analysis course, but assumes no knowledge of device physics whatsoever.

ABOUT INSTRUCTOR :

Prof. Shanthi Pavan obtained the B.Tech degree in Electronics and Communication Engg from the Indian Institute of Technology, Madras in 1995 and the doctoral degree from Columbia University, New York in 1999. Since 2002, he has been with IIT-Madras, where he is now a Chair Professor of Electrical Engineering. His research interests are in the areas of high speed analog circuit design and signal processing.Prof.Pavan is the recipient of several awards, including the IEEE Circuits and Systems Society Darlington Best Paper Award and the Shanti Swarup Bhatnagar Award. He is the author of Understanding Delta-Sigma Data Converters (second edition), with Richard Schreier and Gabor Temes. Prof.Pavan has served as the Editor-in-Chief of the IEEE Transactions on Circuits and Systems:Part I - Regular Papers, and on the technical program committee of the International Solid State Circuits Conference. He has been a Distinguished Lecturer of the Solid-State Circuits and Circuits and Systems Societies. He is a fellow of the Indian National Academy of Engineering, and an IEEE fellow.

COURSE PLAN :

Week 1: Nonlinear-circuit analysis using incremental networks
Week 2: Characteristics of an amplifying nonlinear device; the MOSFET
Week 3: The common-source amplifier: gain and swing limits
Week 4: Robust biasing of transistor amplifiers
Week 5: The incremental VCVS and VCCS using negative feedback
Week 6: The incremental CCVS and CCCS using negative feedback
Week 7: The PMOS transistor, active load and CMOS inverter
Week 8: The differential pair and common-mode rejection ration
Week 9: The basic two-stage opamp; parasitic capacitances in MOS transistors
Week 10: Multi-stage amplifiers in a feedback loop: stability and phase margin
Week 11: Dominant pole compensation of a two-stage opamp, the Miller effect
Week 12: Introduction to BJTs and BJT-based circuits