PHASE LOCKED LOOPS

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PRE-REQUISITES : EE3002 (http://www.ee.iitm.ac.in/vlsi/courses/ee3002_2017/start)

INTENDED AUDIENCE : B.Tech (6th semester onwards), M.Tech./M.S./Ph.D. (1st semester onwards)

INDUSTRY SUPPORT : Texas Instruments, Intel, Qualcomm, Samsung, Cadence

COURSE OUTLINE :

This course will emphasize on developing intuition behind frequency synthesizer design, learning mathematical basis behind operation, and realizing PLLs at architecture and circuit level. The students will be exposed to state-of-the-art frequency synthesis techniques used in analog/digital integer-N PLLs. This course will equip students with skills to analyze, debug, and evaluate a PLL design at analytical and transistor levels both. The students will be able to use their knowledge and skills while generating a clock signal in a power-efficient manner for requirements of a synchronous system.

ABOUT INSTRUCTOR :

Prof. Saurabh Saxena (S'10–M'16) received the B.Tech. degree in electrical engineering, the M.Tech. degree in microelectronics and VLSI design from the Indian Institute of Technology Madras, Chennai, India, in 2009, and the Ph.D. degree in electrical and computer engineering from the University of Illinois, Urbana-Champaign, IL in 2015. He is currently an Assistant Professor in the Department of Electrical Engineering at Indian Institute of Technology Madras, Chennai, India. Prof. Saxena is a recipient of Young Faculty Research Fellowship of Visvesvaraya PhD programme of MeitY, GoI. He serves as a reviewer for the IEEE Journal of Solid-StateCircuits, IEEE Transactions on Circuits and Systems I, IEEE Transactions on Very Large Scale Integration Systems, and IEEE International Symposium on Circuits and Systems. His research interests include delta-sigma modulators, high speed I/O interfaces, and clocking circuits.

COURSE PLAN :

Week 1: Basic concepts in PLL, Simple PLL

Week 2: Small Signal Analysis of Type-I/II/III PLLs for Phase Step, Frequency Step and Frequency Ramp, Frequency acquisition in Type-I PLLs

Week 3: Frequency acquisition in Type-II PLLs, Clock multipliers, Analog phase error detectors

Week 4: Digital phase error detectors, Range extension for phase error detectors, Phase frequency detector, Digital frequency detector, Charge-pump PLL

Week 5: Problems in charge-pump PLL, Design procedure for Type-II Order 3 charge-pump PLL, Design procedure for charge-pump clock multiplier, Sources of non-linearities in CP-PLL, Noise analysis in CP-PLL

Week 6: Noise analysis in CP-PLL (continued), Design of PLL building blocks: Introduction to oscillators

Week 7: Design of PLL building blocks: Ring oscillators

Week 8: Design of PLL building blocks: Ring oscillators (continued), Supply regulated oscillators

Week 9: Phase noise in ring oscillators, Design of PLL building blocks: PFD

Week 10: Design of PLL building blocks: Charge-pump, Circuit-level design of clock frequency divider

Week 11: Techniques for wide frequency range clock multiplier, Digital PLLs

Week 12: Noise analysis in digital PLLs, Analog/Digital Hybrid PLL