High Performance Computer Architecture - Video course

COURSE OUTLINE

Review of Basic Organization and Architectural Techniques

- RISC processors
- Characteristics of RISC processors
- RISC Vs CISC
- Classification of Instruction Set Architectures
- Review of performance measurements
- Basic parallel processing techniques: instruction level, thread level and process level
- Classification of parallel architectures

Instruction Level Parallelism

- Basic concepts of pipelining
- Arithmetic pipelines
- Instruction pipelines
- Hazards in a pipeline: structural, data, and control hazards
- Overview of hazard resolution techniques
- Dynamic instruction scheduling
- Branch prediction techniques
- Instruction-level parallelism using software approaches
- Superscalar techniques
- Speculative execution
- Review of modern processors /*The objective is to explain how ILP

NP-TEL

NPTEL

http://nptel.iitm.ac.in

Computer Science and Engineering

Pre-requisites:

Programming and Data Structures Operating Systems Computer Architecture and Organization.

Additional Reading:

SIMA, “Advanced Computer Architectures”, Addison-Wesley.

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techniques have been deployed in modern processors*/

a. Pentium Processor: IA 32 and P6 microarchitectures

b. ARM Processor

Memory Hierarchies

- Basic concept of hierarchical memory organization
- Main memories
- Cache memory design and implementation
- Virtual memory design and implementation
- Secondary memory technology
- RAID

Peripheral Devices

- Bus structures and standards
- Synchronous and asynchronous buses
- Types and uses of storage devices
- Interfacing I/O to the rest of the system
- Reliability and availability
- I/O system design
- Platform architecture

Thread Level Parallelism

- Centralized vs. distributed shared memory
- Interconnection topologies
- Multiprocessor architecture
- Symmetric multiprocessors
- Cache coherence problem
- Synchronization
- Memory consistency
- Multicore architecture
- Review of modern multiprocessors

Process Level Parallelism

- Distributed computers

- Clusters
- Grid
- Mainframe computers

COURSE DETAIL

Module	Topics	No.of Hours
Review of Basic Organization and Architectural Techniques	RISC processors	6
	Characteristics of RISC processors	
	RISC Vs CISC	
	Classification of Instruction Set Architectures	
	Review of performance measurements	
	Basic parallel processing techniques: instruction level, thread level and process level	
	Classification of parallel architectures	
	Basic concepts of pipelining	
	Instruction pipelines versus functional pipelines	
Instruction Level Parallelism	Basic concepts of pipelining	8

	Arithmetic pipelines	
	Instruction pipelines	
	Hazards in a pipeline: structural, data, and control hazards	
	Overview of hazard resolution techniques	
	Dynamic instruction scheduling	
	Branch prediction techniques	
	Instruction-level parallelism using software approaches	
	Superscalar techniques	
	Speculative execution	
	Review of modern processors /*The objective is to explain how ILP techniques have been deployed in modern processors*/ i. Pentium Processor: IA 32 and P6 microarchitectures ii. ARM Processor	
Memory Hierarchies	Basic concept of hierarchical memory organization	8
	Main memories	
	Cache design and optimization	
	Virtual memory design and	

	implementation	
	Memory protection	
	Evaluating memory hierarchy performance	
	RAID	
Thread Level Parallelism	Centralized vs. distributed shared memory	8
	Interconnection topologies	
	Synchronization	
	Memory consistency	
	Review of modern multiprocessors	
Process Level Parallelism	Distributed computers	6
	Clusters	
	Grid	
	Mainframe computers	
Peripheral Devices	Bus structures and standards	4
	Types and uses of storage devices	
	Interfacing I/O to the rest of the	

	system	
	Reliability and availability	
	I/O system design	

References:

1. Hennessey and Patterson, "Computer Architecture: A quantitative Approach", Morgan Kaufman.