Parallel Computer Architecture - Web course

COURSE OUTLINE

This course is targeted toward post-graduate students with basic understanding of computer organization and architecture.

This course discusses in detail the methodologies and trade-offs involved in designing a shared memory parallel computer.

Contents:

Single-threaded execution, traditional microprocessors, DLP, ILP, TLP, memory wall, parallel programming and performance issues, shared memory multiprocessors, synchronization, small-scale symmetric multiprocessors on a snoopy bus, cache coherence on snoopy buses.

Scalable multiprocessors, directory-based cache coherence, interconnection network, memory consistency models, software distributed shared memory, multithreading in hardware, chip-multiprocessing, current research and future trends.

COURSE DETAIL

Sl.No.	Topics	No.of Hours
1	Introduction to parallel computer architecture, thread-level parallelism (TLP)	2
2	Recap: single-threaded execution	8
3	Recap: virtual memory and caches	4
4	Fundamentals of parallel computers	3
5	Introduction to parallel programming	2
6	Performance issues in parallel program	1
7	Shared memory multiprocessors and cache coherence	6
8	Synchronization	4
9	Design of shared memory multiprocessors I: Multiprocessors on a snoopy bus	6
10	Design of shared memory multiprocessors II:	4

NP-TEL

NPTEL

http://nptel.iitm.ac.in

Computer Science and Engineering

Pre-requisites:

Undergraduate computer organization and architecture.

Coordinators:

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	Scalable multiprocessors and directory-based cache coherence	
11	Memory consistency models	-
12	Software distributed shared memory multiprocessors	2
13	Interconnection networks	8
14	Simultaneous multithreading and chip-multiprocessing	4
15	Research direction	3

References:

1. D. E. Culler and J. P. Singh with A. Gupta. Parallel Computer Architecture. Morgan- Kaufmann publishers.
2. J. L. Hennessy and D. A. Patterson. Computer Architecture: A Quantitative Approach. Morgan-Kaufmann publishers.