VLSI Design Verification and Test - Web course

COURSE OUTLINE

Digital VLSI Design flow comprises three basic phases: Design, Verification and Test. The web course would cover theoretical, implementation and CAD tools pertaining to these three phases.

Although there can be individual full courses for each of these phases, the present course aims at covering the important problems/algorithms/tools so that students get a comprehensive idea of the whole digital VLSI design flow.

VLSI Design: High level Synthesis, Verilog RTL Design, Combinational and Sequential Synthesis Logic Synthesis (for large circuits).

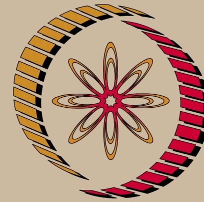
Verification Techniques: Introduction to Hardware Verification and methodologies, Binary Decision Diagrams(BDDs) and algorithms over BDDs.

Combinational equivalence checking, Temporal Logics, Modeling sequential systems and model checking, Symbolic model checking.

VLSI Testing: Introduction, Fault models, Fault Simulation, Test generation for combinational circuits, Test generation algorithms for sequential circuits and Built in Self test.

COURSE DETAIL

Title	Sl.No.	Module/Lecture
Design	I	**Introduction**
	1	Introduction to Digital VLSI Design Flow Specification, High level Synthesis, RTL Design, Logic Optimization, Verification and Test Planning
	2	Design Representation
	3	Hardware Specific Transformations
	II	**Scheduling, Allocation and Binding**
	1	Problem Specification: Scheduling, Allocation and Binding
	2	Basic Scheduling Algorithms (Time constrained and Resource Constrained)
	3	Allocation Steps: Unit Selection, Functional Unit Binding, Storage Binding, Interconnect Binding



NPTEL

http://nptel.iitm.ac.in

Computer Science and Engineering

Pre-requisites:

1. Digital Design
2. Algorithm
3. Automata Theory (Basics)

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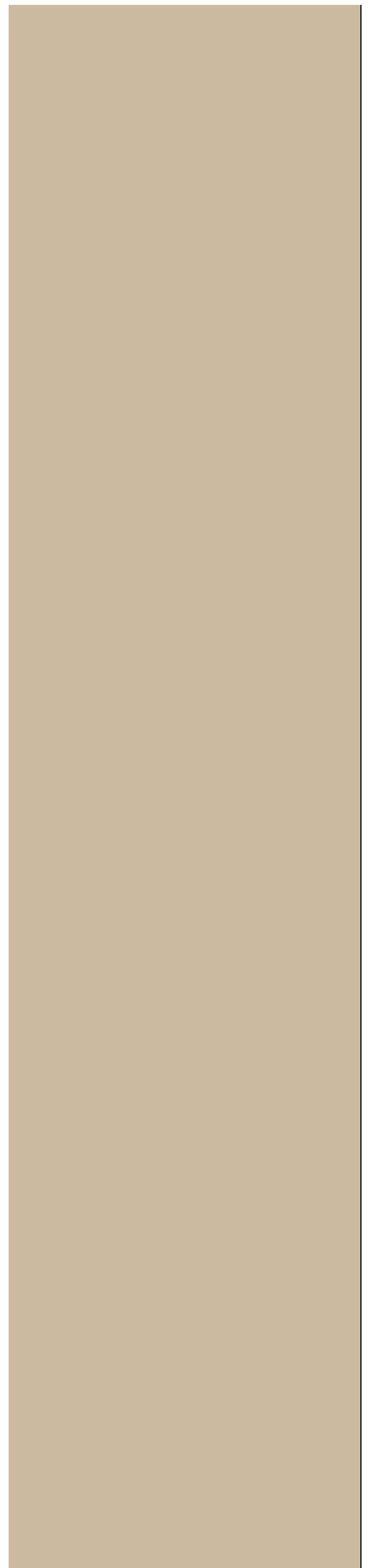
	4	Allocation Techniques: Clique Partitioning, Left-Edge Algorithm, Iterative Refinement.
	III	**Logic Optimization and Synthesis**
	1	Heuristic Minimization of Two-Level Circuits: Espresso
	2	Finite State Machine Synthesis
	3	Multi-Level Logic Synthesis
	4	Multi-Level Minimization
	5	Technology Mapping
Verification	IV	**Binary Decision Diagram**
	1	Introduction and construction
	2	Reduction rules and Algorithms, ROBDDs
	3	Operation on BDDs and its Algorithms
	4	Representation of Sequential Circuits
	V	**Temporal Logic**
	1	Introduction and Basic Operators
	2	Syntax and Semantics of LTL, CTL and CLT*
	3	Equivalence and Expressive Power
	VI	**Model Checking**
	1	Introduction to Verification
	2	Specification and Modelling
	3	Model Checking Algorithm

	4	Symbolic Model Checking	
	5	Automata and its use in Verification	
	6	Automata Theoretic Model Checking	
	7	Practical Examples with SMV	
Test	VII	**Introduction to Digital Testing**	
	1	Introduction, Test process and Test economics	
	2	Functional vs. Structural Testing Defects, Errors, Faults and Fault Modeling (mainly stuck at fault modeling)	
	3	Fault Equivalence, Fault Dominance, Fault Collapsing and Checkpoint Theorem	
	VIII	**Fault Simulation and Testability Measures**	
	1-2	Circuit Modeling and Algorithms for Fault Simulation • Serial Fault Simulation • Parallel Fault Simulation • Deductive Fault Simulation • Concurrent Fault Simulation	
	3	Combinational SCOAP Measures and Sequential SCOAP Measures	
	IX	**Combinational Circuit Test Pattern Generation**	
	1	Introduction to Automatic Test Pattern Generation (ATPG) and ATPG Algebras	
	2	Standard ATPG Algorithms • D-Calculus and D-Algorithm • Basics of PODEM and FAN	
	X	**Sequential Circuit Testing and Scan Chains**	
	1	ATPG for Single-Clock Synchronous Circuits • Use of Nine-Valued Logic and Time-Frame Expansion Methods	

		• Complexity of Sequential ATPG
	2-3	Scan Chain based Sequential Circuit Testing • Scan Cell Design • Design variations of Scan Chains • Sequential Testing based on Scan Chains • Overheads of Scan Design • Partial-Scan Design
	XI	**Built in Self test (BIST)**
	1	Introduction to BIST architecture BIST Test Pattern Generation, Response Compaction and Response Analysis
	2-3	Memory BIST • March Test • BIST with MISR • Neighborhood Pattern Sensitive Fault Test • Transparent Memory BIST

References:

1. D. D. Gajski, N. D. Dutt, A.C.-H. Wu and S.Y.-L. Lin, High-Level Synthesis: Introduction to Chip and System Design, Springer, 1st edition, 1992.
2. S. Palnitkar, Verilog HDL: A Guide to Digital Design and Synthesis, Prentice Hall, 2nd edition, 2003.
3. G. De Micheli. Synthesis and optimization of digital circuits, 1st edition, 1994.
4. M. Huth and M. Ryan, Logic in Computer Science modeling and reasoning about systems, Cambridge University Press, 2nd Edition, 2004.
5. Bushnell and Agrawal, Essentials of Electronic Testing for Digital, Memory & Mixed-Signal Circuits, Kluwer Academic Publishers, 2000.