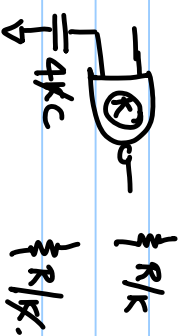
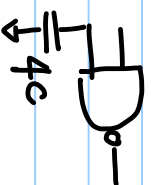
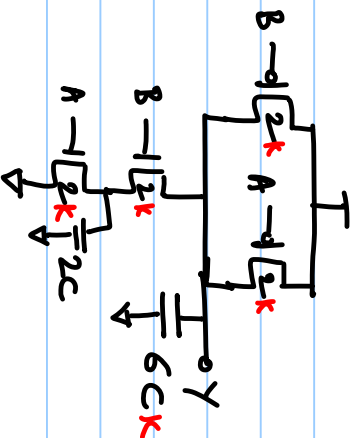


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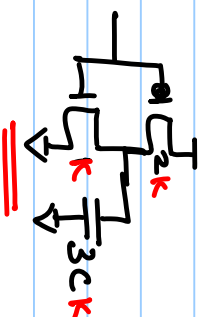
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MODULE-4: COMBINATIONAL CIRCUITS

PARASITIC DELAY

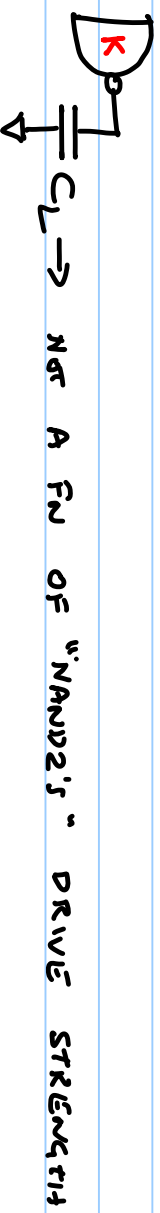


Delay $7RC/6k$

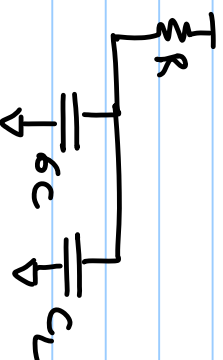
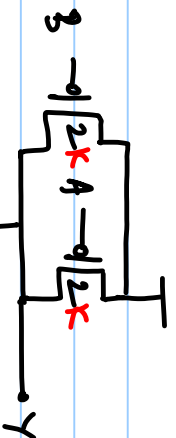


$$p = \frac{6C}{3C} = 2$$

DRIVING A LOAD CAPACITANCE

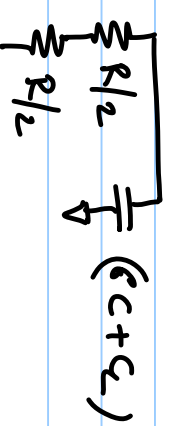


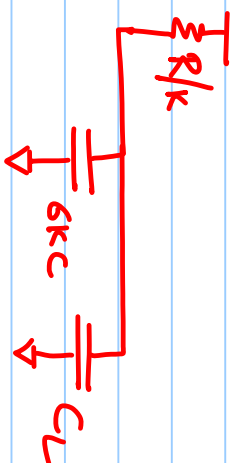
RISE PROP DELAY:



$$\text{Rise delay} = R \cdot (C_C + C_L)$$

$$\text{Fall delay} = R(C_C + C_L)$$





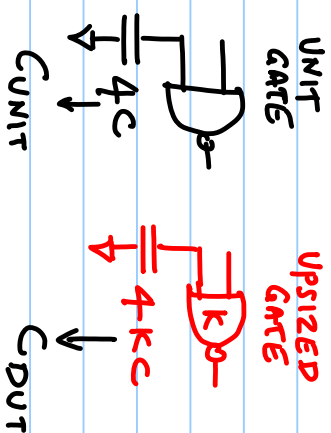
$$\text{Rise delay} = \frac{R}{k} (6kC + C_L)$$

$$= \underbrace{6kC}_{\text{Parasitic delay}} + \underbrace{\frac{R \cdot C_L}{k}}_{\text{Load delay term}}$$

$$\text{Fall delay} = \frac{R}{k} (6kC + C_L)$$

$$= \underbrace{6kC}_{\text{Parasitic delay}} + \underbrace{\frac{R \cdot C_L}{k}}_{\text{Load delay term}}$$

$$\frac{R \cdot C_L}{k}$$

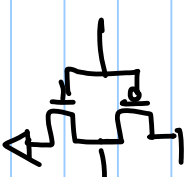


$$k = \frac{C_{DUT}}{C_{UNIT}}$$

Parasitic delay.
Load delay term

$$\frac{R \cdot C_L}{K} = \frac{R \cdot C_L \cdot (C_{UNIT})}{(C_{OUT})} = R \cdot \left(\frac{C_L}{C_{OUT}} \right) \cdot C_{UNIT}$$

$$\text{delay} = R \left(\frac{C_L}{C_{OUT}} \right) \cdot C_{UNIT} + n R C$$



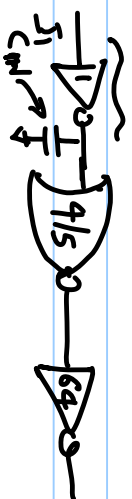
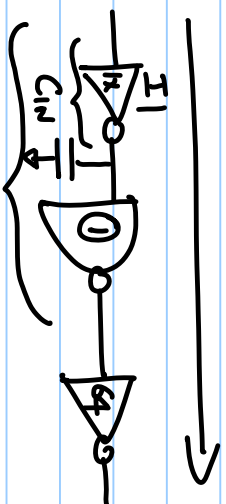
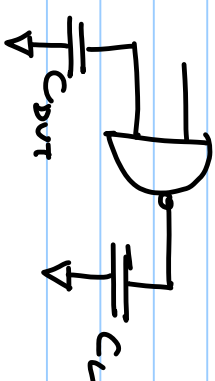
Normalised delay : $\text{delay} \div \text{delay of a ref unit inv} = 3RC$

$$\hat{d} = \left(R \cdot \left(\frac{C_L}{C_{OUT}} \right) \cdot C_{UNIT} + n R C \right) / 3RC$$

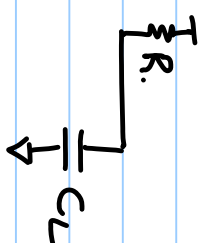
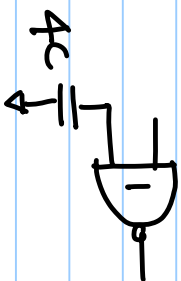
$$= \underbrace{\left(\frac{C_L}{C_{OUT}} \right) \cdot \left(\frac{C_{UNIT}}{3C} \right)} + \left(\frac{n}{3} \right)$$

$$\left(\frac{C_L}{C_{DUT}}\right) \cdot \left(\frac{C_{UNIT}}{3C}\right)$$

ELECTRICAL EFFORT LOGICAL EFFORT } PURELY A FN OF THE LOGIC TOPOLOGY

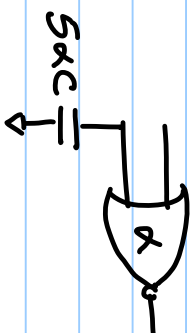


PATH delay = $d_{I_1} + d_{DUT}$ (d_{NAND} OR d_{NOR})
 delay of I_1 should be same



($C_L \gg C_{PAR}$)

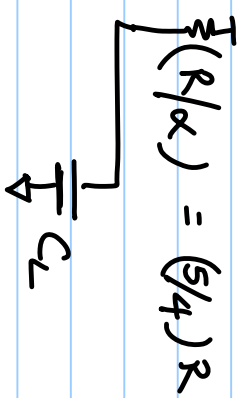
$$d_{aur} = R C_L$$



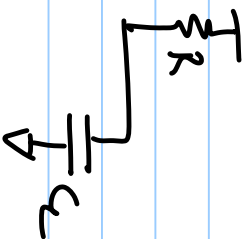
\Rightarrow

$$5\alpha C = 4C$$

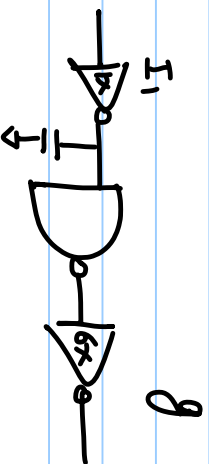
$$\therefore \alpha = \frac{4}{5}$$



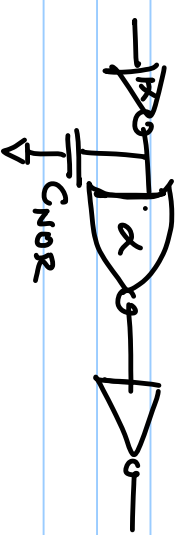
$$d_{aur} = \frac{5}{4} R \cdot C_L$$



$$d_{\text{delay}} = \left(\frac{C_L}{C_{\text{OUT}}} \right) \cdot \left(\frac{C_{\text{UNIT}}}{C_{\text{INV}}} \right) + p. \leftarrow$$



$$\overline{dI_1} = \left(\frac{C_{\text{NAND}}}{C_{\text{IX}}} \right) \cdot +$$



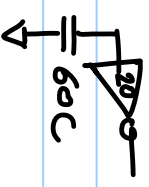
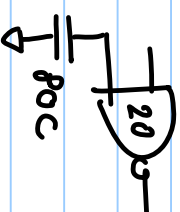
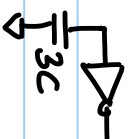
$$\overline{dI_1} = \left(\frac{C_{\text{NOR}}}{C_{\text{IX}}} \right) \cdot$$

$$\overline{d_{\text{NAND}}} = \left(\frac{C_{\text{INVEG}}}{C_{\text{NAND}}} \right) \cdot \left(\frac{C_{\text{UNIT}}}{C_{\text{INV}}} \right) +$$

$$\overline{d_{\text{NOR}}} = \left(\frac{C_{\text{INVEG}}}{C_{\text{NOR}}} \right) \cdot \left(\frac{C_{\text{UNIT-NOR}}}{C_{\text{INV}}} \right) + \dots$$

LOGICAL EFFORT = g = RATIO OF GATE CAP OF THE GATE (DUT) TO
 GATE CAP OF A STATIC CMOS INVERTER WITH
SAME DRIVE STRENGTH.

NAND3:



$$g = \frac{5}{3}$$

$$\therefore g = \frac{4}{3}$$



$$g = \frac{1}{3}$$

