Unit 8 - VLSI Testing [Part-2]

Assignment for Week 6

The due date for submitting this assignment has passed. **Due on 2018-03-21, 23:59 IST.**

Submitted assignment

1) Compatible bits in test patterns are mainly used for ***1 point***

- Test Pattern elimination
- Test Pattern verification
- Test Pattern compression
- All the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
Test Pattern compression

2) Generally speaking, for tester memory optimization, input test vectors are _____ and responses are _____ ***1 point***

- Compressed, compacted
- Compacted, Compressed
- Compressed, Compressed
- Compacted, Compacted

No, the answer is incorrect.
Score: 0

Accepted Answers:
Compressed, compacted

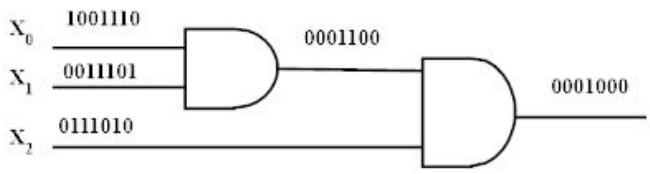
3) Test Stimulus Compression based on linear operations are performed by ***1 point***

- LFSR
- XOR network
- Neither (a) nor (b)
- Both (a) and (b)

No, the answer is incorrect.
Score: 0

Accepted Answers:
Both (a) and (b)

4) Consider the circuit given below. The output is compacted using transition count. What is the value of transition count at the output? ***1 point***



- 1
- 2
- 3
- 4

No, the answer is incorrect.
Score: 0

Accepted Answers:
2

5) "If stuck-then fault" model is mainly applicable for **1 point**

- Gate level testing
- RTL testing
- Transistor level testing
- Not considered as a fault model

No, the answer is incorrect.
Score: 0

Accepted Answers:
RTL testing

6) Huffman compression is a code based compression method, which can be applied on test patterns. Which are true about Huffman compression method? **1 point**

i. High frequency pattern is given lower width.
ii. High frequency pattern is given higher width.
iii. Root corresponds to the lowest frequency pattern.
iv. Root corresponds to the highest frequency pattern.

- ii and iii are true.
- i and iii are true.
- Only iii is true.
- i and iv are true.

No, the answer is incorrect.
Score: 0

Accepted Answers:
i and iv are true.

7) Select the false statements about scan chain. **1 point**

i. Parallel scan can reduce test clock cycles with increase in number of I/Os.
ii. Parallel scan increases test clock cycles but reduces the number of I/Os.
iii. If a FF if it is difficult to control or depth is high it should be scan enabled.
iv. Scan chain increases no of multiplexers but reduces testing complexity.

- ii and iii are false.
- Only ii is false.
- iii and iv are false.
- Only i is false.

No, the answer is incorrect.
Score: 0

Accepted Answers:
Only ii is false.

8) Select the false statement about High level fault modeling and RTL based testing. **1 point**

- High level fault modeling improves test coverage and reliability.
- With help of High level fault models, computational complexity of ATPG is addressed.
- High level fault modeling and RTL based testing are better suited for large circuits like NoC.
- There exists good co-relation between high level fault models and gate level fault models.

No, the answer is incorrect.
Score: 0

Accepted Answers:
High level fault modeling improves test coverage and reliability.

9) What kind of fault is represented by the following high level fault model code segments? **1 point**

Code:1

```
Primary input=X,Y;
Primary Output=OUT1;
IF ( X< Y) THEN
OUT1 <= “1”;
 ELSE
OUT1 <= “1”;
END IF;
```

Code:2

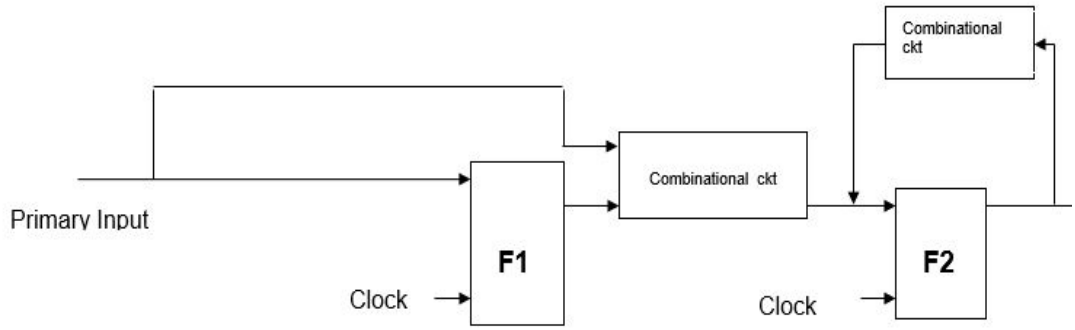
```
IF (TRUE)
 THEN A <= IN1;
ElSE-IF (logical_expression2)
THEN A <= IN2;
ELSE
A <= IN3;
END IF;
```

- “If stuck then fault” and “input stuck at 1” fault, respectively.
- “Input stuck at 1” fault and “if stuck then fault”, respectively.
- “Bridging fault” and “stuck at zero” fault, respectively.
- “Stuck at zero” fault and “bridging fault”, respectively.

No, the answer is incorrect.
Score: 0

Accepted Answers:
“Input stuck at 1” fault and “if stuck then fault”, respectively.

10)What method is best suited for testing the given circuit? ***1 point***



- Full Scan chain method (Single Scan chain comprising F1 and F2).
- Parallel scan chain method (Separate Scan chains for F1 and F2).
- Time Frame based testing (F1 and F2 are not scan enabled).
- Partial scan chain (F2 is scan enabled and F1 is not Scan enabled).

No, the answer is incorrect.
Score: 0

Accepted Answers:
Partial scan chain (F2 is scan enabled and F1 is not Scan enabled).

Previous Page End