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Unit 7 - VLSI Testing [Part-1]

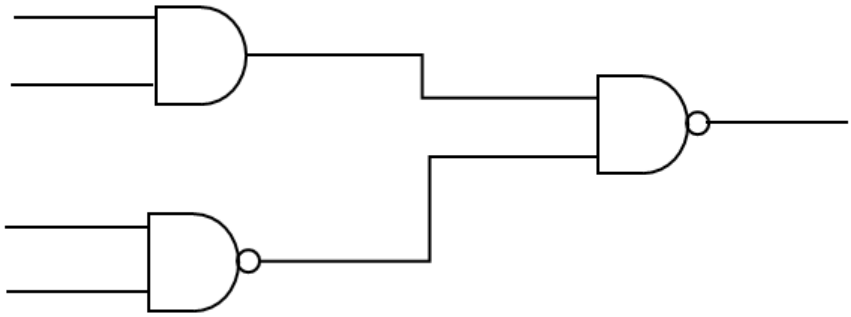
Assignment for Week 5

The due date for submitting this assignment has passed. **Due on 2018-03-14, 23:59 IST.**

Submitted assignment

Assignments on introduction to VLSI testing

1) How many single stuck at-0 faults are possible in the given circuit? ***1 point***



- 4
- 2
- 7
- 6

No, the answer is incorrect.
Score: 0

Accepted Answers:
7

2) Which one is false about functional testing? ***1 point***

- Not feasible for large scale systems.
- Not feasible, as it demands very long duration of test time for a complex circuit.
- Not feasible as the number required test patterns is very high for real life circuits.
- Not feasible due to low accuracy/coverage of faults.

No, the answer is incorrect.
Score: 0

Accepted Answers:
Not feasible due to low accuracy/coverage of faults.

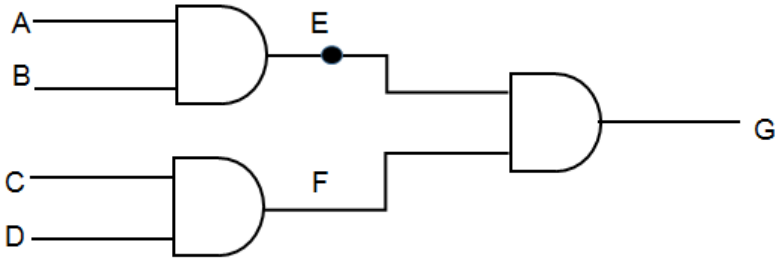
3) The procedure to generate a test input for a given a fault is called _____. ***1 point***

- Test Procedure Generation
- Test Pattern Generation
- Test Parameter Generation
- None

No, the answer is incorrect.
Score: 0

Accepted Answers:
Test Pattern Generation

4) To detect S-A-0 at E in the figure, using path sensitization based automatic test pattern generation (ATPG), fault activation can be done as, ***1 point***

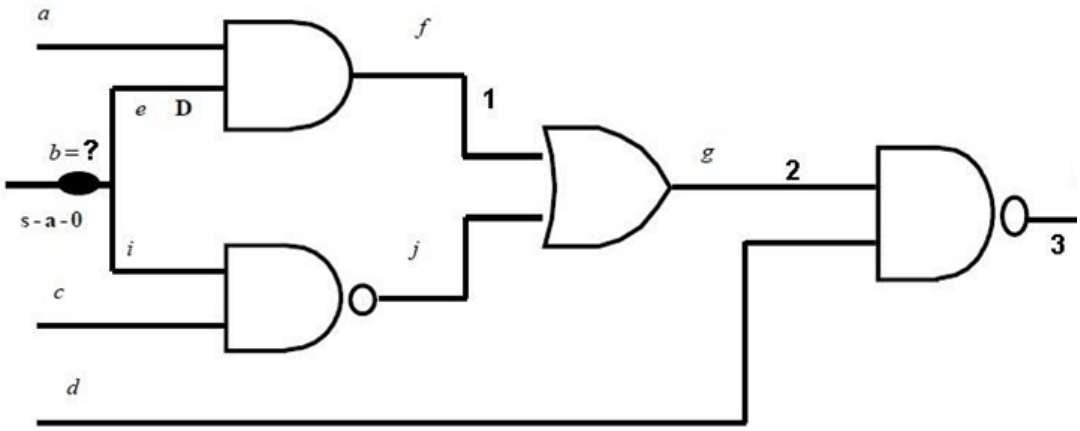


- Sensitization by E = 0.
- Sensitization by E = 1.
- Justification by F = 0.
- Justification by A = 0.

No, the answer is incorrect.
Score: 0

Accepted Answers:
Sensitization by E = 1.

5) Let one want to take the path "e-f-g-h" (shown below) for propagating the fault effect to the output h. The signal value of the net labeled with 1 (i.e., f) is _____. ***1 point***

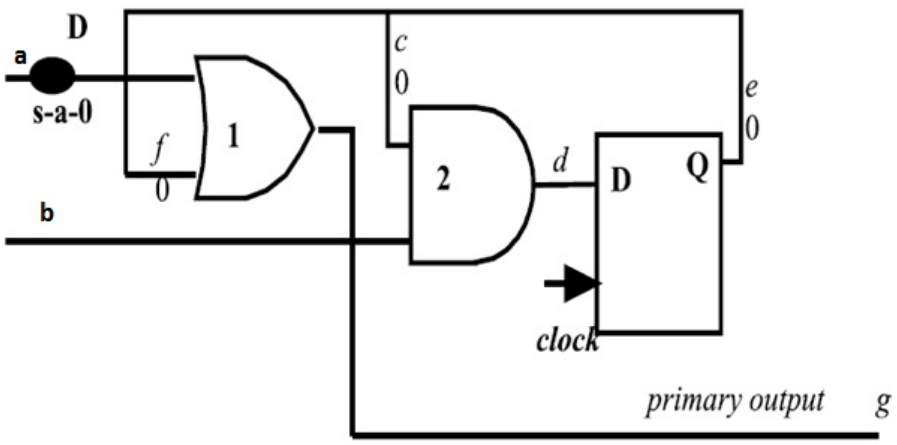


- 0
- 1
- D
- X

No, the answer is incorrect.
Score: 0

Accepted Answers:
D

6) Consider the circuit and the s-a-0 fault shown in the figure. The input pattern(s) to test the fault is (are) _____. ***1 point***



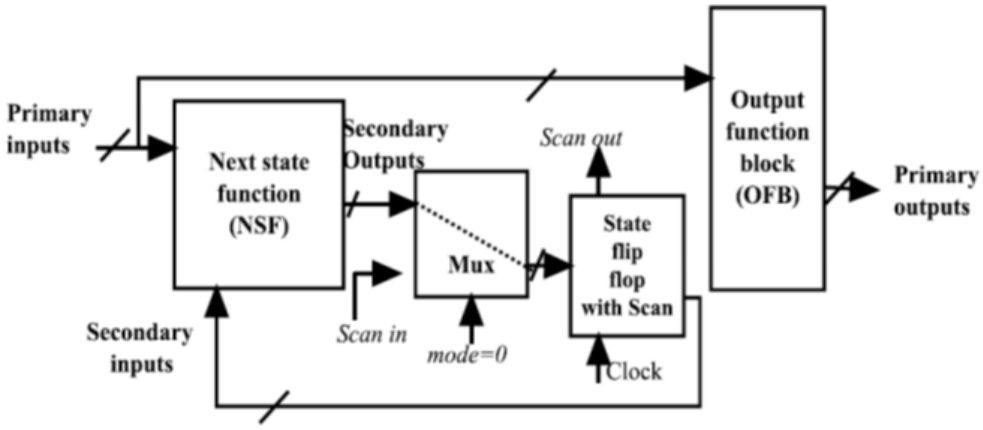
- a=X and b=0
- a=1 and b=X

- a=1 and b=X followed by a clock edge and then a=X, b=0
- a=X, b=0 followed by a clock edge and then a=1 and b=X

No, the answer is incorrect.
Score: 0

Accepted Answers:
a=X, b=0 followed by a clock edge and then a=1 and b=X

7) Consider a block diagram of a sequential circuit shown above. Which of the following is true? ***1 point***



- The circuit has Scan chain and is in scan chain (test) mode
- The circuit has Scan chain and is in normal (functional) mode
- The circuit does not have scan chain
- The circuit has scan chain but is permanently disabled

No, the answer is incorrect.
Score: 0

Accepted Answers:
The circuit has Scan chain and is in normal (functional) mode

8) There is a bridging AND fault between net 1 and net 2, where signal 1 and 0 applied, respectively. There is a bridging OR fault between net 3 and net 4, where signal 1 and signal 0 applied respectively. Choose the correct statements. ***1 point***

i. Net 1 will dominate net 2 and present a S-A-0 fault at net 2.
ii. Net 3 will dominate net 4 and present a S-A-1 fault at net 4.
iii. Net 4 will dominate net 3 and present a S-A-0 fault at net 4.
iv. Net 2 will dominate net 1 and present a S-A-0 fault at net 1.

- Only iii is correct.
- ii and iv are correct.
- i and ii are correct.
- Only iv is correct.

No, the answer is incorrect.
Score: 0

Accepted Answers:
ii and iv are correct.

9) Choose the correct statements about delay fault. ***1 point***

i. For testing delay to rise fault, we actually test S-A-0 fault at speed.
ii. For testing delay to rise fault, we actually test S-A-1 fault at speed.
iii. Testing delay fault can cover all possible stuck at faults.
iv. Testing delay fault is expensive, as test pattern need to be applied at high speed.

- Only ii and iv are true.
- Only iii is true.
- Only ii, iv are true.
- Only i, iii and iv are true.

No, the answer is incorrect.
Score: 0

Accepted Answers:
Only i, iii and iv are true.

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