X

Unit 6 - Logic Synthesis and Physical Synthesis

Assignment for Week 4

The due date for submitting this assignment has passed. **Due on 2018-03-07, 23:59 IST.**

Submitted assignment

1) Find the essential prime implicants of the following Boolean function. ***1 point***

F = a'bc + ab'c + abc + abc'

- bc, ab, bc'
- bc, ab, ac
- bc', ab, a'c'
- bc, ab', ac

No, the answer is incorrect.
Score: 0

Accepted Answers:
bc, ab, ac

2) Which one of the following cubes is a kernel of the function F = abc + abd + bcd? ***1 point***

- abc + abd + bcd
- bc + bd
- ac + ad + cd
- None of the above.

No, the answer is incorrect.
Score: 0

Accepted Answers:
ac + ad + cd

3) Which one of the following statement is NOT correct about Boolean functions? ***1 point***

- Boolean function can be implemented with only prime implicants.
- Essential prime implicant covers a minterm that is not covered by any other prime implicant.
- An irredundant cover is a cover that is not a proper superset of any cover.
- Don't care is an input combination that may or may not occur.

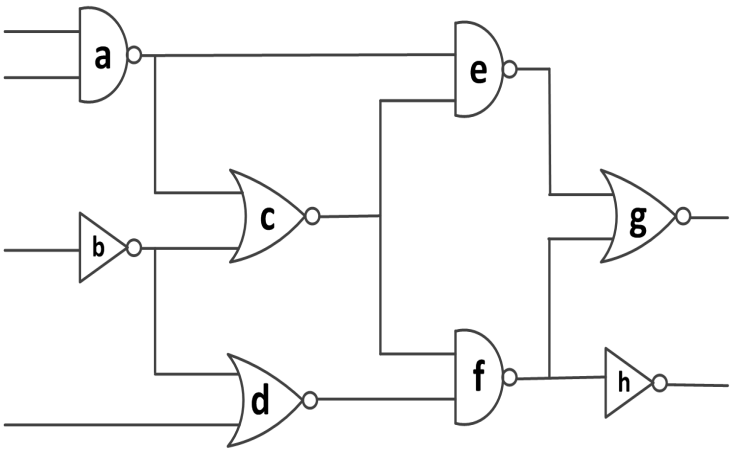
No, the answer is incorrect.
Score: 0

Accepted Answers:
Don't care is an input combination that may or may not occur.

4) Consider the following gate level design. Find the minimum 4 input LUTs required to implement it in FPGA? ***1 point***

Verification [Part-1]

Verification [Part-2]



- 2
- 3
- 4
- None of the above.

No, the answer is incorrect.
Score: 0

Accepted Answers:
2

5) Which of the following statements are correct? ***1 point***

- One of the objectives of routing problem is to minimize total wire length.
- Details of I/O pin positions are fixed during floor planning.
- Channel routing operation attempts to maximize channel width.
- None of the above.

No, the answer is incorrect.
Score: 0

Accepted Answers:
One of the objectives of routing problem is to minimize total wire length.

6) Let us assume that data path width is such that multiplier can be mapped to DSP block of FPGA. Which of the following statement is correct about DSP mapping? ***1 point***
S1: A multiplier with a pre-adder can be mapped to a single DSP.
S2: An accumulator for each multiplier cannot be mapped to a single DSP. The accumulator will be mapped to LUTs and the multiplier will be mapped to DSP block.

- S1
- S2
- S1 and S2
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
S1

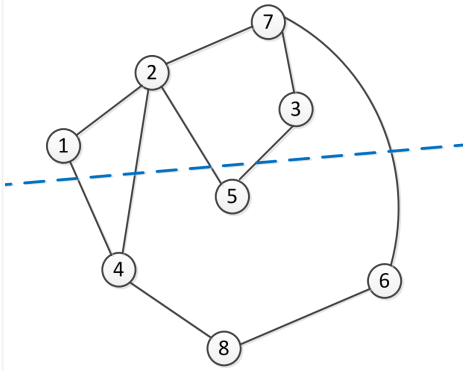
7) Which of the following statements are correct? ***1 point***

- Nodes in critical paths have the luxury to select different cuts.
- A node with high fanouts is a good choice as an internal node of a cut.
- A node with high fanouts is good choice as a root node of a cut
- All of the above.

No, the answer is incorrect.
Score: 0

Accepted Answers:
A node with high fanouts is good choice as a root node of a cut

8) Consider the graph with initial partition shown through the cut line. After application of one iteration of the inner loop of Kernighan-Lin (KL) algorithm on this circuit results in the final cut with size is ___. Assume that each edge weight is one. ***1 point***



- 5
- 4
- 3
- 2

No, the answer is incorrect.
Score: 0

Accepted Answers:
3

9) For the graph in question 8, the partition resulting from KL algorithm is, ***1 point***

- Partition 1: {1, 4, 6, 8}; Partition 2: {2, 3, 5, 7}
- Partition 1: {1, 2, 3, 8}; Partition 2: {4, 5, 6, 7}
- Partition 1: {1, 2, 3, 4}; Partition 2: {5, 6, 7, 8}
- None of the above.

No, the answer is incorrect.
Score: 0

Accepted Answers:
Partition 1: {1, 4, 6, 8}; Partition 2: {2, 3, 5, 7}

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