Unit 5 - RTL Optimizations [Part-2]

Assignment for Week 3

The due date for submitting this assignment has passed. **Due on 2018-02-28, 23:59 IST.**

Submitted assignment

1) Given a system of M inequalities in N variables where each inequality has the form ri –rj <= k, k is an integer, shortest path algorithm can be used to solve them. The constraint graph is obtained as follows: ***1 point***

1. Draw the node i for each of the N variables ri, i = 1, 2, 3, … , N.
2. Draw node N + 1.
3. For each inequality ri –rj <= k, draw the edge j -> i, from j to i of length k.
4. For each node i, i = 1, 2, 3, … , N, draw the edge N+1 -> i from node N+1 to i with length 0.

Consider the following graph in figure-1. What will be inequalities for this graph?

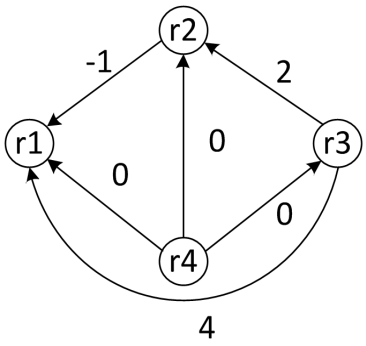

Figure-1

- r1 – r2 <= -1; r2 – r3 <= 2; r1 – r3 <= 4;
- r1 – r2 <= 1; r2 – r3 <= -2; r1 – r3 <= -4;
- r2 – r1 <= -1; r3 – r2 <= 2; r3 – r1 <= 4;
- r1 – r4 <= 1; r2 – r4 <= 2; r3 – r4 <= 0;

No, the answer is incorrect.
Score: 0

Accepted Answers:
r1 – r2 <= -1; r2 – r3 <= 2; r1 – r3 <= 4;

2) In question 1, what would be the values of r1, r2 and r3? ***1 point***

- r1 = -1, r2 = 0, r3 = 1
- r1 = -1, r2 = 0, r3 = 0
- r1 = 1, r2 = 0, r3 = 0
- None of the above

Verification [Part-2]

No, the answer is incorrect.
Score: 0

Accepted Answers:
r1 = -1, r2 = 0, r3 = 0

3) Which one of the following statements is correct regarding circuit representation graph? ***1 point***
S1: Every cycle in the graph has at least one register.
S2: Number of registers in each edge can be negative.

- S1
- S2
- Both S1 and S2
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
S1

4) Consider the graph representing digital circuit in figure-2. The number associated with the node is the computation delay of that node. The number associated with the edge is the number of registers in that edge. Let W(u, v) be the minimum number of registers on all paths between u and v. Let D(u, v) be the maximum delay on all paths between u and v with minimum number of registers. What would be the value of W(u, v) and D(u, v) for the graph in figure 2? ***1 point***

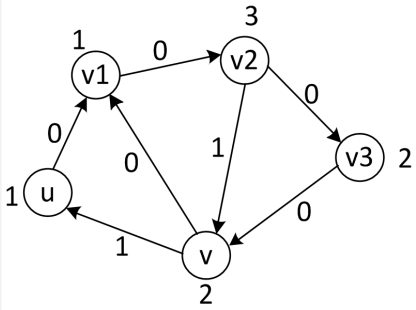

Figure-2

- D(p) = 9, W(p) = 1
- D(p) = 7, W(p) = 1
- D(p) = 9, W(p) = 0
- D(p) = 7, W(p) = 0

No, the answer is incorrect.
Score: 0

Accepted Answers:
D(p) = 9, W(p) = 0

5) Which of the following statements is correct about area optimization? ***1 point***
S1: Rolling up the pipeline can optimize the area
S2: Folding is a useful technique for area optimization

- S1
- S2
- Both S1 and S2
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
Both S1 and S2

6) Passing signals between two different clock domains cause of metastability. Which of the following technique can be used to avoid metastability? ***1 point***

- Retiming
- Replication
- Pipelining
- Double flopping

No, the answer is incorrect.
Score: 0

Accepted Answers:
Double flopping

7) During FPGA prototyping of design targeted for ASIC, the gated clock conversion (GCC) is used. Which one of the following statement is true about GCC? ***1 point***

- GCC is used to move enable signals cone to the data path or enable cone of logic of sequential loads to the clock tree
- GCC is used to move enable signals from clock tree cone to the data path or enable cone of logic of sequential loads
- GCC is not used during FPGA prototyping of ASIC design
- GCC is used to reduce the power requirement of a design

No, the answer is incorrect.
Score: 0

Accepted Answers:
GCC is used to move enable signals from clock tree cone to the data path or enable cone of logic of sequential loads

8) Consider the following Verilog code. How many block RAM will be inferred from this code? Assume that register memdat [0:255] can be mapped to single block RAM. ***1 point***

```
module resetckt(
    output reg [15:0] oDat,
    input iReset, iClk, iWrEn,
    input [7:0] iAddr, oAddr,
    input [15:0] iDat);
    reg [15:0] memdat [0:255];
    always @(posedge iClk or negedge iReset)
    if(!iReset)
        oDat <= 0;
    else begin
        if(iWrEn)
            memdat[iAddr] <= iDat;
        oDat <= memdat[oAddr];
    end
endmodule
```

- 0
- 1
- 2
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
0

9) Consider the following Verilog code. How many block RAM will be inferred from this code? Assume that register memdat [0:255] can be mapped to single block RAM. ***1 point***

```
module resetckt(
    output reg [15:0] oDat,
    input iReset, iClk, iWrEn,
    input [7:0] iAddr, oAddr,
    input [15:0] iDat);
```

```
    reg [15:0] memdat [0:255];
    always @(posedge iClk)
    if(!iReset)
        oDat <= 0;
    else begin
        if(iWrEn)
            memdat[iAddr] <= iDat;
        oDat <= memdat[oAddr];
    end
endmodule
```

- 0
- 1
- 2
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
1

10) Which of the following statement is NOT true about folding transformation? ***1 point***

- Folding creates multiple synchronous clocks
- Folding increases register and MUX counts
- Folding of two functional units in series creates a feedback loop.
- Folding of two functional units in parallel creates a feedback loop.

No, the answer is incorrect.
Score: 0

Accepted Answers:
Folding of two functional units in parallel creates a feedback loop.

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