

X

NPTEL

reviewer1@nptel.iitm.ac.in ▼

Courses » Optimization Techniques for Digital VLSI Design

Announcements Course Ask a Question Progress Mentor

Unit 1 - How to access the portal

Course outline

How to access the portal

- Lesson 1: How to access the home page?
- Lesson 2: How to access the course page?
- Lesson 3: How to access the MCQ, MSQ and Programming assignments?
- Quiz : Assignment for Week 0

Introduction and High-level Synthesis [Part-1]

Introduction and High-level Synthesis [Part-2]

RTL Optimizations [Part-1]

RTL Optimizations [Part-2]

Logic Synthesis and Physical Synthesis

VLSI Testing [Part-1]

VLSI Testing [Part-2]

Assignment for Week 0

The due date for submitting this assignment has passed. **Due on 2018-01-20, 00:00 IST.**

Submitted assignment

1) How many full adders and half adders are required to construct an m-bit parallel adder? **1 point**

- m/2 full adders and m/2 half adders
- m half adders
- m-1 full adders and 1 half adder
- m+1 half adders

No, the answer is incorrect.

Score: 0

Accepted Answers:

m-1 full adders and 1 half adder

2) How many types of flip-flops are generally used? **1 point**

- 2
- 3
- 4
- 5

No, the answer is incorrect.

Score: 0

Accepted Answers:

4

3) How many inputs and outputs does a D flip-flop has (excluding the clock) **1 point**

- 2 inputs and 2 outputs
- 1 input and 2 outputs
- 1 input and 1 output
- None of the above

No, the answer is incorrect.

Score: 0

Accepted Answers:

1 input and 2 outputs

4) A clock with frequency X (MHZ) is applied to a cascaded counter containing a modulus-4 counter, a modulus-8 counter, and a modulus-10 counter. The lowest output frequency possible is **1 point**

- X/4 MHz
- X/8 MHz

Verification [Part-1]

Verification [Part-2]

- X/32 MHz
- X/320 MHz

No, the answer is incorrect.
Score: 0

Accepted Answers:
X/320 MHz

5) Which of the following describes most appropriately a “shift register”

1 point

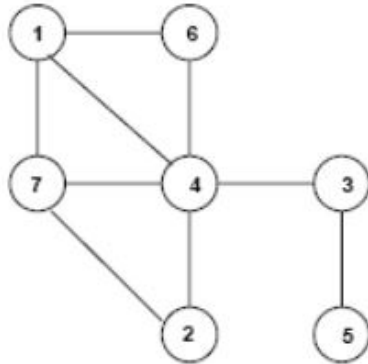
- The register that can shift information bits to another register
- The register that can shift information bits either to the right or to the left
- The register that can shift information bits to the right only
- The register that can shift information bits to the left only

No, the answer is incorrect.
Score: 0

Accepted Answers:
The register that can shift information bits either to the right or to the left

6) What is the chromatic number of the following graph?

1 point



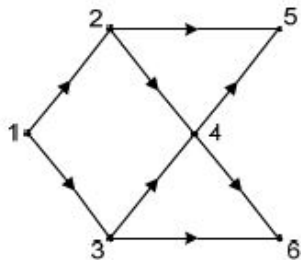
- 1
- 2
- 3
- 4

No, the answer is incorrect.
Score: 0

Accepted Answers:
3

7) Consider the DAG with $V = \{1, 2, 3, 4, 5, 6\}$ below. Which one the following is NOT a topological ordering?

1 point



- 1 2 3 4 5 6
- 1 3 2 4 5 6
- 1 3 2 4 6 5
- 3 2 4 1 6 5

No, the answer is incorrect.

Score: 0

Accepted Answers:

3 2 4 1 6 5

8) To achieve linear time complexity of Dijkstra's shortest path algorithm on undirected and unweighted graphs, the data structure to be used is

1 point

- Queue
- Stack
- Heap
- B-Tree

No, the answer is incorrect.

Score: 0

Accepted Answers:

Queue

9) A Language for which a DFA can be constructed is a _____

1 point

- Regular Language
- Context free Language
- Recursively enumerable language
- None of the above

No, the answer is incorrect.

Score: 0

Accepted Answers:

Regular Language

10) In the formal definition of a deterministic finite state machine the number of tuples required is

1 point

- 4
- 5
- 6
- 7

No, the answer is incorrect.

Score: 0

Accepted Answers:

5

You were allowed to submit this assignment only once.

Previous Page

End

Funded by

Government of India
Ministry of Human Resource Development

Powered by

