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Courses » Parallel Algorithms

Announcements

Course

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Unit 2 - Week 01: Models of Computation

Register for
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Course outline

How to access the portal

Week 01: Models of Computation

- Lecture 1:
Shared
Memory
Models - 1
- Lecture 2:
Shared
Memory
Models - 2
- Lecture 3:
Interconnection
Networks

Quiz :
Assessment 1

Week 02: Performance of parallel algorithms, Basic techniques

Week 03: Basic Techniques

Week 04: Comparator Networks; List Colouring

Week 05: An

Assessment 1

The due date for submitting this assignment has passed.

As per our records you have not submitted this **Due on 2019-02-13, 23:59 IST.**
assignment.

1) In a step of a PRAM, processors P1 through P9 want to read from locations 4, 8, 14, 35, **1 point**
20, 92, 14, 7, 6, and write into locations 9, 54, 3, 56, 27, 64, 18, 96, 92, respectively. If the PRAM is of
the EREW variety, which of the following statements is true?

- (i) Processor P9 reads location 6
- (ii) Processor P9 writes into location 92
- (iii) The program crashes

- only (i)
- only (ii)
- only (iii)
- both (i) and (ii)

No, the answer is incorrect.

Score: 0

Accepted Answers:

only (iii)

2) In a step of a PRIORITY CRCW PRAM, processors P1 through P9 want to write values 8, **1 point**
12, 13, 11, 91, 13, 12, 11, 12 into locations 9, 54, 3, 54, 27, 54, 18, 96, 92, in which the values at
present are 22, 8, 13, 8, 13, 8, 13, 10, 9, respectively. What is the value in location 54, after the step?

- cannot say
- 11
- 12
- 13

No, the answer is incorrect.

Score: 0

Accepted Answers:

12

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Ranking algorithm, Expression Tree Evaluation, Merging and Cole's Merge Sort

Week 07: Cole's Merge Sort, Sorting Lower Bound, Connected Components

Week 08: Connected Components, Vertex Colouring and Interconnection Networks Algorithms

Week 09: Interconnection Networks Algorithms

Interaction Session

Week 10: Interconnection Networks Algorithms

Week 11: Interconnection Networks Algorithms

Week 12: Parallel Complexity Theory

12 for certain

13 for certain

No, the answer is incorrect.

Score: 0

Accepted Answers:

cannot say

4) In a step of a COMMON CRCW PRAM, processors P1 through P9 want to write values 8, 12, 13, 11, 91, 13, 12, 11, 12 into locations 9, 54, 3, 54, 27, 54, 18, 96, 92, in which the values at present are 22, 8, 13, 8, 13, 8, 13, 10, 9, respectively. What is the value in location 54, after the step?

cannot say

the program crashes

12 for certain

13 for certain

No, the answer is incorrect.

Score: 0

Accepted Answers:

the program crashes

5) In a step of a TOLERANT CRCW PRAM, processors P1 through P9 want to write values 8, 12, 13, 11, 91, 13, 12, 11, 12 into locations 9, 54, 3, 54, 27, 54, 18, 96, 92, in which the values at present are 22, 8, 13, 8, 13, 8, 13, 10, 9, respectively. What is the value in location 54, after the step?

8 for certain

11 for certain

12 for certain

13 for certain

No, the answer is incorrect.

Score: 0

Accepted Answers:

8 for certain

6) A step of a COLLISION CRCW PRAM can be simulated on an ARBITRARY CRCW PRAM in _____ steps.

2

3

4

5

No, the answer is incorrect.

Score: 0

Accepted Answers:

3

7) When an algorithm designed for TOLERANT CRCW PRAM is simulated on a COLLISION CRCW PRAM, the space requirement goes up by a factor of _____.

2

3

4

5

No, the answer is incorrect.

Score: 0

Accepted Answers:

2

8) The OR of n bits can be found in $O(1)$ time on a/an _____ PRAM. **1 point**

- CREW
- EREW
- PRIORITY CRCW
- None of the above



No, the answer is incorrect.

Score: 0

Accepted Answers:

PRIORITY CRCW

9) Which of the following models is more powerful than TOLERANT CRCW PRAM? **1 point**

- ARBITRARY CRCW
- COMMON CRCW
- CREW
- EREW

No, the answer is incorrect.

Score: 0

Accepted Answers:

COMMON CRCW

10) Which of the following models is more powerful than COMMON CRCW PRAM? **1 point**

- PRIORITY CRCW
- COLLISION
- CREW
- EREW

No, the answer is incorrect.

Score: 0

Accepted Answers:

PRIORITY CRCW

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