



Unit 9 - Introduction to Digital Testing

Course outline

How to access the portal

Introduction and Modeling

Modeling and Synthesis issues

Architectural Synthesis of Hardwares

System-level Design

Temporal Logic

Model Checking

BDD and Symbolic Model Checking

Introduction to Digital Testing

- Introduction to Digital VLSI Testing
- Automatic Test Pattern Generation (ATPG)
- Quiz : Assignment-8

Embedded System Hardware Testing

Embedded System Hardware Testing - II

Advances in Embedded System Hardware Testing

Advances in Embedded System Hardware Testing - II

Assignment-8

The due date for submitting this assignment has passed. As per our records you have not submitted this assignment.

Due on 2018-09-26, 23:59 IST.

1) Murphy's Law states that _____

1 point

- If anything can go wrong, it will
- If nothing goes wrong, it will
- If anything can go wrong, it will not
- If nothing goes wrong, it will not

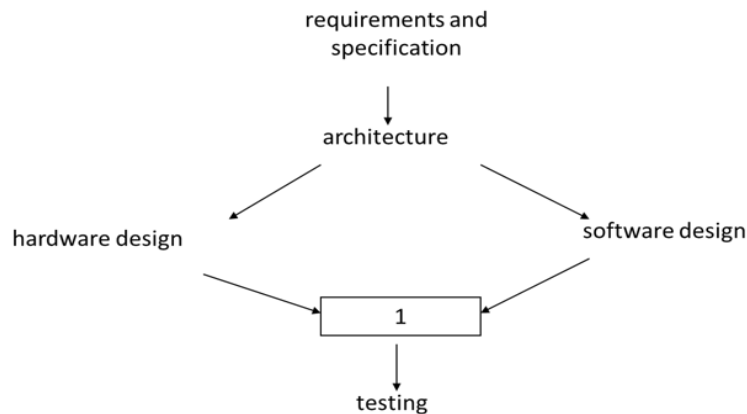
No, the answer is incorrect.

Score: 0

Accepted Answers:

If anything can go wrong, it will

2) Figure below illustrates the process of Embedded Systems Design and Test flow. What is the block marked "1" in the figure? 1 point



- Test Response storage
- Integration
- Test Response compressor
- Copy of Manufactured circuit under test

No, the answer is incorrect.

Score: 0

Accepted Answers:



- Data flow-based testing
- None

No, the answer is incorrect.

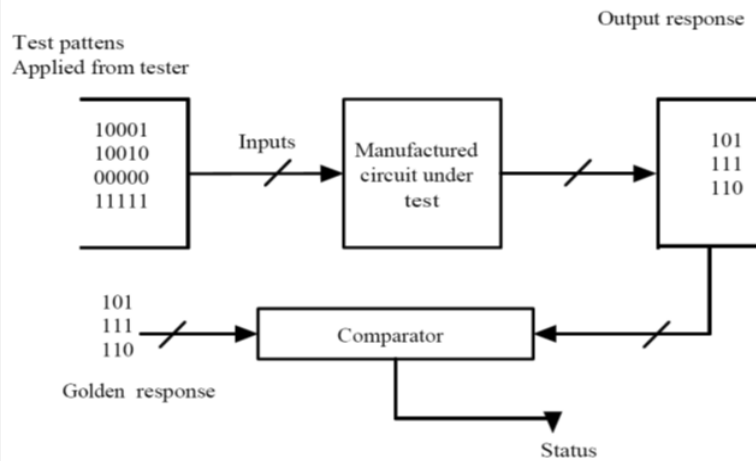
Score: 0

Accepted Answers:

Design for testability

4) Figure below illustrates a process of ____ circuit testing.

1 point



- Digital
- Analog
- Both of the above
- None of the above

No, the answer is incorrect.

Score: 0

Accepted Answers:

Digital

5) For an n-input circuit, ____ test patterns are needed for functional testing.

1 point

- n
- 2n
- n²
- 2ⁿ

No, the answer is incorrect.

Score: 0

Accepted Answers:

2ⁿ

6) A circuit with n nets can have ____ possible stuck-at faults under single stuck-at fault model.

1 point

- 2ⁿ
- n²
- infinite
- 2n

No, the answer is incorrect.

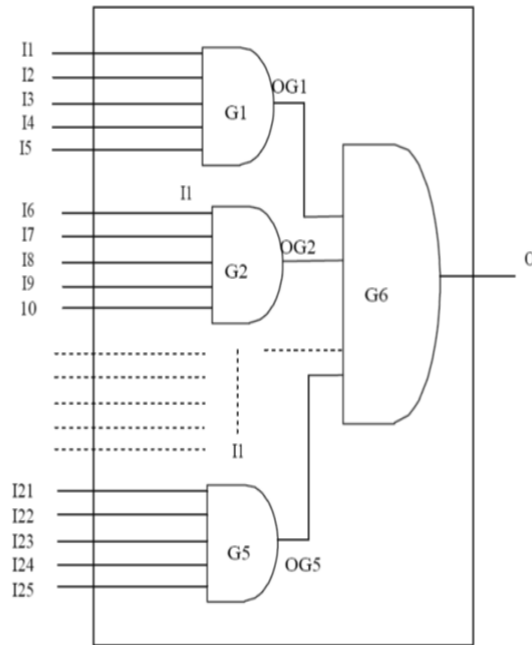
Score: 0

Accepted Answers:

2n

7) How many test patterns are needed to test the circuit given in the figure below? Assume that structural testing with single stuck at fault model is used.

0 points



- 25
- 60
- 192
- 160

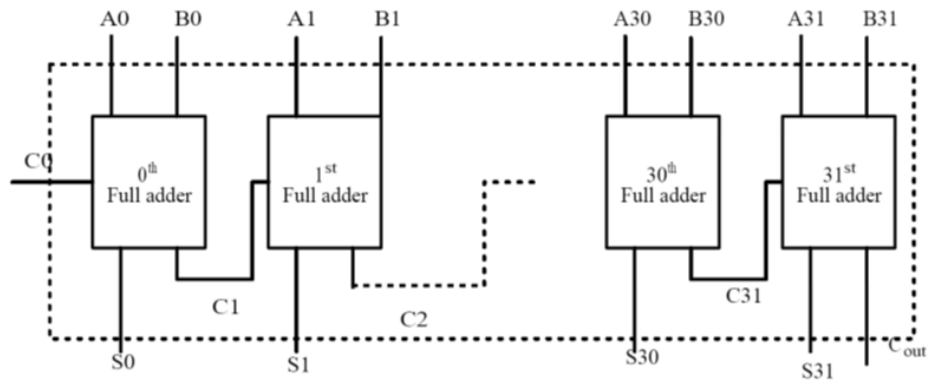
No, the answer is incorrect.

Score: 0

Accepted Answers:

192

8) Functional and structural testing of the 32-Bit adder circuit shown below needs ____ and ____ test patterns, **1 point** respectively.



- $2^{65}, 2^3$
- $2 * 65, 2^3$
- $2^{65}, 2 * 3$
- 65, 3

No, the answer is incorrect.

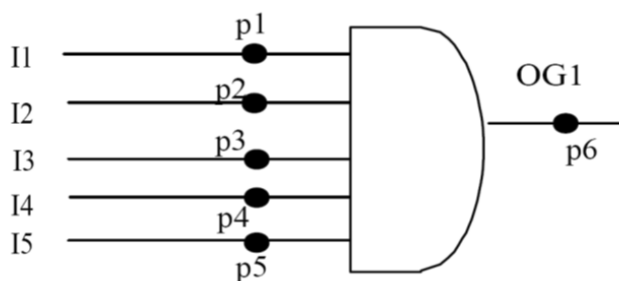
Score: 0

Accepted Answers:

$2^{65}, 2^3$

9) How many stuck-at faults are possible in the AND-gate shown below?

1 point



- 6
- 12
- 11
- 10

No, the answer is incorrect.

Score: 0

Accepted Answers:

12

10)A net having fan-out to k gates will have ___ stuck at fault locations

1 point

- k+1
- k-1
- 2k
- None

No, the answer is incorrect.

Score: 0

Accepted Answers:

k+1

11)Which of the following statement is generally valid for a circuit?

1 point

- All faults are "easy to test"
- All faults are "difficult to test"
- Few faults are "easy to test" and most others are "difficult to test"
- Most faults are "easy to test" and few are "difficult to test"

No, the answer is incorrect.

Score: 0

Accepted Answers:

Most faults are "easy to test" and few are "difficult to test"

12)The test patterns for "easy to test faults" are derived by ___

1 point

- Fault simulation algorithms
- Sensitization-propagation -justification approach
- Boolean Difference approach
- All the above

No, the answer is incorrect.

Score: 0

Accepted Answers:

Fault simulation algorithms

13)The test patterns for "difficult to test faults" are derived by ___

1 point

- Fault simulation algorithms
- Sensitization-propagation -justification approach
- both (a) and (b)
- other than the above

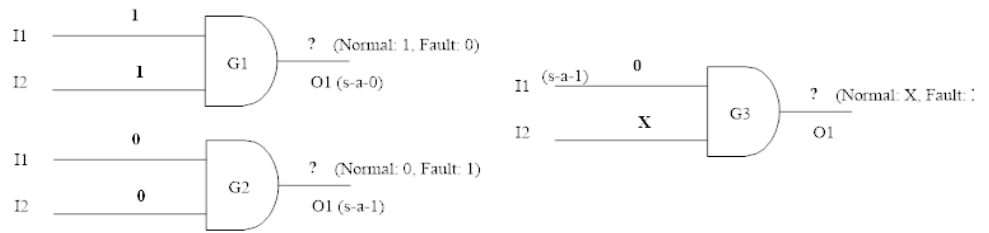
No, the answer is incorrect.

Score: 0

Accepted Answers:

Sensitization-propagation-justification approach

14) Let us consider a 2-input AND gates shown in figure below where the inputs are marked using notations from Roth's 5-valued algebra. What is the output notation at the ? marked net i.e., output of gate G1? **1 point**



- 0
- 1
- D
- X

No, the answer is incorrect.

Score: 0

Accepted Answers:

D

15) Consider figure of Question 14. What is the output notation at the ? marked net i.e., output of gate G2? **1 point**

- 0
- \bar{D}
- D
- X

No, the answer is incorrect.

Score: 0

Accepted Answers:

\bar{D}

16) Consider figure of Question 14. What is the output notation at the ? marked net i.e., output of gate G3? **1 point**

- 0
- D
- 1
- X

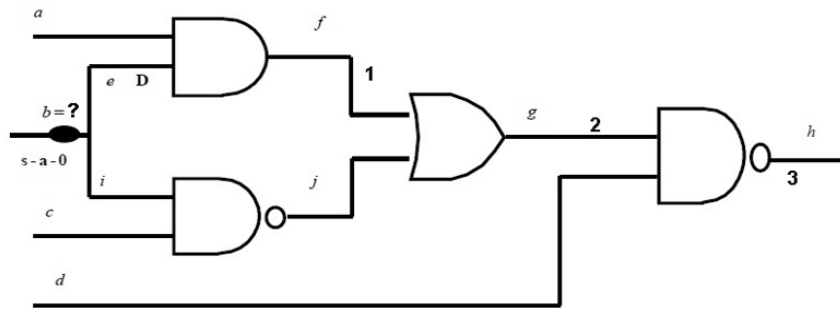
No, the answer is incorrect.

Score: 0

Accepted Answers:

X

17) If one wants to take the path "e-f-g-h" in the figure below for propagating the fault effect to the output h. The signals labelled as 1, 2, 3 in the nets of the path are assigned in terms of Roth's 5 valued algebra. The signal value of the net labelled with 1 is _____.



- 0
- 1
- D
- X

No, the answer is incorrect.

Score: 0

Accepted Answers:

D

Previous Page

End