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reviewer3@nptel.iitm.ac.in ▼

Courses » Embedded Systems-- Design Verification and Test

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Unit 4 - Architectural Synthesis of Hardwares

Course outline

How to access the portal

Introduction and Modeling

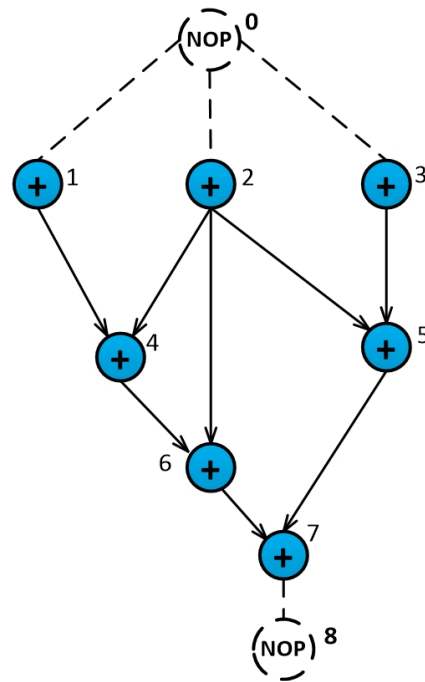
Modeling and Synthesis issues

Architectural Synthesis of Hardwares

- Hardware Architectural Synthesis – 1
- Hardware Architectural Synthesis – 2
- Hardware Architectural Synthesis – 3
- Hardware Architectural Synthesis – 4
- Hardware Architectural Synthesis – 5
- Hardware Architectural Synthesis – 6
- Hardware Architectural Synthesis – 7

Assignment-3

The due date for submitting this assignment has passed. As per our records you have not submitted this assignment. **Due on 2018-09-05, 23:59 IST.**



Consider the Operation Constraints Graph (OCG) shown in the figure above. Each addition operation takes unit time. The latency bound is 4. There are no resource constraints.

1) The correct ALAP schedule is: **1 point**

- C-step 1: 1, 2. C-step 2: 3, 4. C-step 3: 5, 6. C-step 4: 7
- C-step 1: 1, 2, 3. C-step 2: 4, 5. C-step 3: 6. C-step 4: 7

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Temporal Logic	ce De	<i>C-step 1: 1, 2. C-step 2: 3, 4. C-step 3: 5, 6. C-step 4: 7</i>	1 point
Model Checking		2) The mobility for each node (from 1 to 7) in OCG is: <input type="radio"/> 0, 1, 0, 0, 0, 1, 0 <input type="radio"/> 0, 1, 1, 0, 1, 0, 0 <input type="radio"/> 0, 0, 1, 0, 1, 0, 0 <input type="radio"/> 0, 0, 1, 0, 1, 1, 0	
BDD and Symbolic Model Checking		<p>No, the answer is incorrect. Score: 0 Accepted Answers: 0, 0, 1, 0, 1, 0, 0</p>	
Introduction to Digital Testing		3) A valid list schedule for the OCG assuming only one adder resource is: (Note: Assume the priority of a operation as (1 / (mobility + 1))). <input type="radio"/> 1, 2, 4, 6, 3, 5, 7 <input type="radio"/> 1, 2, 3, 4, 5, 6, 7 <input type="radio"/> 1, 2, 4, 3, 6, 5, 7 <input type="radio"/> 1, 2, 3, 5, 4, 6, 7	1 point
Embedded System Hardware Testing		<p>No, the answer is incorrect. Score: 0 Accepted Answers: 1, 2, 4, 6, 3, 5, 7</p>	
Embedded System Hardware Testing - II		4) A new addition (+) operation having index-9 has been introduced to the OCG. This newly included operation takes the output of operations 1 and 3 as input and floats its output on operation 7. What will be minimum number of resources (i.e., adders) required to schedule this modified OCG with a latency bound of 4. <input type="radio"/> 1 <input type="radio"/> 2 <input type="radio"/> 3 <input type="radio"/> 4	1 point
Advances in Embedded System Hardware Testing		<p>No, the answer is incorrect. Score: 0 Accepted Answers: 3</p>	
Advances in Embedded System Hardware Testing - II		5) Consider the modified OCG discussed in Q4. Let binary decision variables of type $x(i,j)$ denote the assignment of operation- i at time step- j . $x(i,j)$ is 1 if operation- i is scheduled at time step- j . $x(i,j)$ is 0 otherwise. There are two adders and latency bound is 5. Determine the correct inequality representing the resource constraint at time step 2. <input type="radio"/> $x(3,2) + x(4,2) + x(5,2) + x(9,2) \leq 2$ <input type="radio"/> $x(1,2) + x(2,2) + x(3,2) + x(4,2) + x(5,2) \leq 2$ <input type="radio"/> $x(1,2) + x(2,2) + x(3,2) + x(4,2) + x(5,2) + x(9,2) \leq 2$ <input type="radio"/> $x(1,2) + x(2,2) + x(3,2) + x(4,2) + x(5,2) + x(9,2) + x(6,2) \leq 2$	3 points
Testing for Embedded Software Systems		<p>No, the answer is incorrect. Score: 0 Accepted Answers: $x(1,2) + x(2,2) + x(3,2) + x(4,2) + x(5,2) + x(9,2) \leq 2$</p>	

6) Consider the modified OCG discussed in Q4 and Q5. Determine the correct inequality representing the dependency constraint between operations 9 and 3. **3 points**

- $x(9,2) + x(9,3) - x(3,1) - x(3,2) \geq 1$
- $x(9,2) + x(9,3) + x(9,4) - x(3,1) - x(3,2) - 3x(3,3) - 1 \geq 0$
- $2x(9,2) + 3x(9,3) + 4x(9,4) - x(3,1) - 2x(3,2) - 3x(3,3) \geq 0$
- $2x(9,2) + 3x(9,3) + 4x(9,4) - x(3,1) - 2x(3,2) - 3x(3,3) \geq 1$

No, the answer is incorrect.

Score: 0

Accepted Answers:

$2x(9,2) + 3x(9,3) + 4x(9,4) - x(3,1) - 2x(3,2) - 3x(3,3) \geq 1$

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