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Courses » Embedded Systems-- Design Verification and Test

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Unit 10 - Embedded System Hardware Testing

Course outline

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Introduction and Modeling

Modeling and Synthesis issues

Architectural Synthesis of Hardwares

System-level Design

Temporal Logic

Model Checking

BDD and Symbolic Model Checking

Introduction to Digital Testing

Embedded System Hardware Testing

- Scan Chain based Sequential Circuit Testing (Contd. from Previous Module)
- Software-Hardware

Assignment-9

The due date for submitting this assignment has passed. **Due on 2018-10-03, 23:59 IST.**
As per our records you have not submitted this assignment.

1) To test the sequential circuits, the number of test patterns are required in time frame expansion method is: ***1 point***

- No. of primary inputs
- d_{seq}+ 1
- $2^{\text{No. of primary inputs}}$
- 1

No, the answer is incorrect.
Score: 0

Accepted Answers:
d_{seq}+ 1

2) Which of the following is **TRUE** about the testing of sequential circuits? ***1 point***

- Test pattern generation is complicated than of combinational circuits.
- Multiple number of test patterns are required.
- If the output of a flip-flop can be controlled by only primary inputs, its sequential depth is 1
- All of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
All of the above

3) With set/reset flip-flops, how many patterns are required to test a fault in sequential circuits? ***1 point***

- 1
- d_{seq} + 1
- 2
- d_{seq}

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Quiz : Assignment-9

Embedded System Hardware Testing - II

Advances in Embedded System Hardware Testing

Advances in Embedded System Hardware Testing - II

Testing for Embedded Software Systems

- A requirement of a package of thousands of I/O pins, which makes it impractical.
- A shift register is used and loads itself with the pattern required for setting the flip-flops
- Only 3 extra I/O lines are required for testing a fault
- Both b & c are TRUE

No, the answer is incorrect.
Score: 0

Accepted Answers:
Both b & c are TRUE

5) Which of the following is not among the three new I/Os added for ATPG Set and reset by shift register? ***1 point***

- S_clock
- S_in
- test in
- test out

No, the answer is incorrect.
Score: 0

Accepted Answers:
S_in

6) Which of the following is **FALSE** for Scan Chain based Testing? ***1 point***

- The flip-flops in the circuit are converted under test itself to a shift register
- Area overhead for testing is huge
- In test mode, the flip-flops are decoupled from the circuit and they are connected in form of a shift register
- if there are n_{ff} flip-flops, then n_{ff} clock pulses are required to set/reset the flip-flops

No, the answer is incorrect.
Score: 0

Accepted Answers:
Area overhead for testing is huge

7) High level fault models for RTL must be: ***1 point***

- Convenient representation of the effect of the physical defects or failures
- Well-correlated with the physical defects of the circuit
- Test schemes of higher description level to improve the scalability
- All of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
All of the above

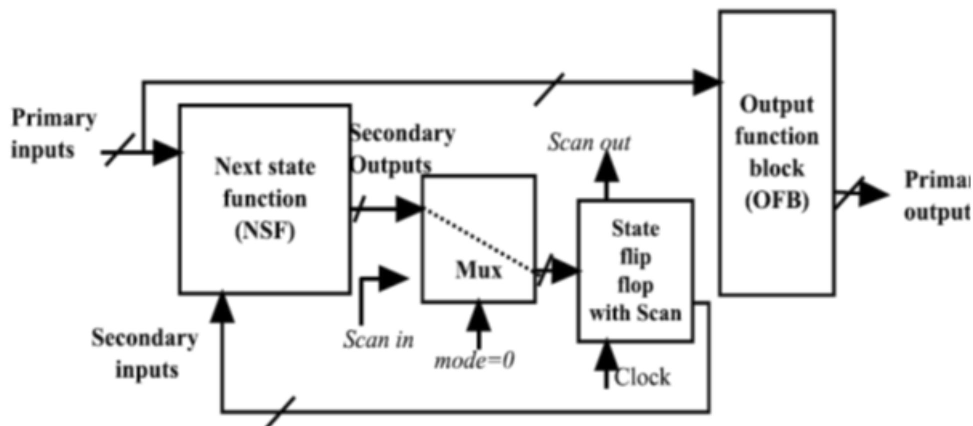
8) For High level fault models for RTL: ***1 point***

- Number of test patterns required is higher than structural testing
- Minimizes test pattern generation time
- Higher accuracy than gate-level fault models are ensured
- All of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
Minimizes test pattern generation time

9) For the sequential circuit shown below, Which of the following is TRUE? ***1 point***



- The circuit has Scan chain and is in functional mode
- The circuit does not have scan chain
- The circuit has scan chain but is permanently disabled
- The circuit has Scan chain and is in test mode

No, the answer is incorrect.
Score: 0

Accepted Answers:
The circuit has Scan chain and is in functional mode

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