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NPTEL

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Courses » Embedded Systems-- Design Verification and Test

Announcements **Course** Ask a Question Progress Mentor FAQ

Unit 1 - How to access the portal

Course outline

How to access the portal

- How to access the home page?
- How to access the course page?
- How to access the MCQ, MSQ and Programming assignments?
- Quiz : Assignment-00

Introduction and Modeling

Modeling and Synthesis issues

Architectural Synthesis of Hardwares

System-level Design

Temporal Logic

Model Checking

BDD and

Assignment-00

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment.

Due on 2018-07-29, 23:59 IST.

1) How many full adders and half adders are required to construct an m-bit parallel adder? ***1 point***

- m/2 full adders and m/2 half adders
- m half adders
- m-1 full adders and 1 half adder
- m+1 half adders

No, the answer is incorrect.
Score: 0

Accepted Answers:
m-1 full adders and 1 half adder

2) How many types of flip-flops are generally used? ***1 point***

- 2
- 3
- 4
- 5

No, the answer is incorrect.
Score: 0

Accepted Answers:
4

3) How many inputs and outputs does a D flip-flop has (excluding the clock) ***1 point***

- 2 inputs and 2 outputs
- 1 input and 2 outputs

4) A clock with frequency X (MHZ) is applied to a cascaded counter containing a modulus-4 counter, a modulus-8 counter, and a modulus-10 counter. The lowest output frequency possible is _____ ***1 point***

- X/4 MHz
- X/8 MHz
- X/32 MHz
- X/320 MHz

No, the answer is incorrect.
Score: 0

Accepted Answers:
X/320 MHz

5) Which of the following describes most appropriately a “shift register”? ***1 point***

- The register that can shift information bits to another register
- The register that can shift information bits either to the right or to the left
- The register that can shift information bits to the right only
- The register that can shift information bits to the left only

No, the answer is incorrect.
Score: 0

Accepted Answers:
The register that can shift information bits either to the right or to the left

6) Which among the following is the queue that keeps the processes that are residing in main memory and are ready and waiting to be executed? ***1 point***

- job queue
- ready queue
- execution queue
- process queue

No, the answer is incorrect.
Score: 0

Accepted Answers:
ready queue

7) Which of the scheduling algorithms mentioned below works by allocating the CPU first to the process that requests the CPU first? ***1 point***

- first-come, first-served scheduling
- shortest job scheduling
- priority scheduling
- none of the mentioned

No, the answer is incorrect.
Score: 0

Accepted Answers:
first-come, first-served scheduling

8) One of the following statements best describes the disadvantage of priority based scheduling algorithm ***1 point***

- Complex Scheduler in terms of computation

- Schedule takes a lot of time
- May lead to some low priority process waiting indefinitely for the CPU
- none of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
May lead to some low priority process waiting indefinitely for the CPU

9) A Language for which a DFA can be constructed is a_____ ***1 point***

- Regular Language
- Context free Language
- Recursively enumerable language
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
Regular Language

10) In the formal definition of a deterministic finite state machine the number of tuples required is ***1 point***

- 4
- 5
- 6
- 7

No, the answer is incorrect.
Score: 0

Accepted Answers:
5

Previous Page End