Phase locked loop frequency synthesizers

Analog Integrated Circuit Design
A video course under the NPTEL

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National Programme on Technology Enhanced Learning

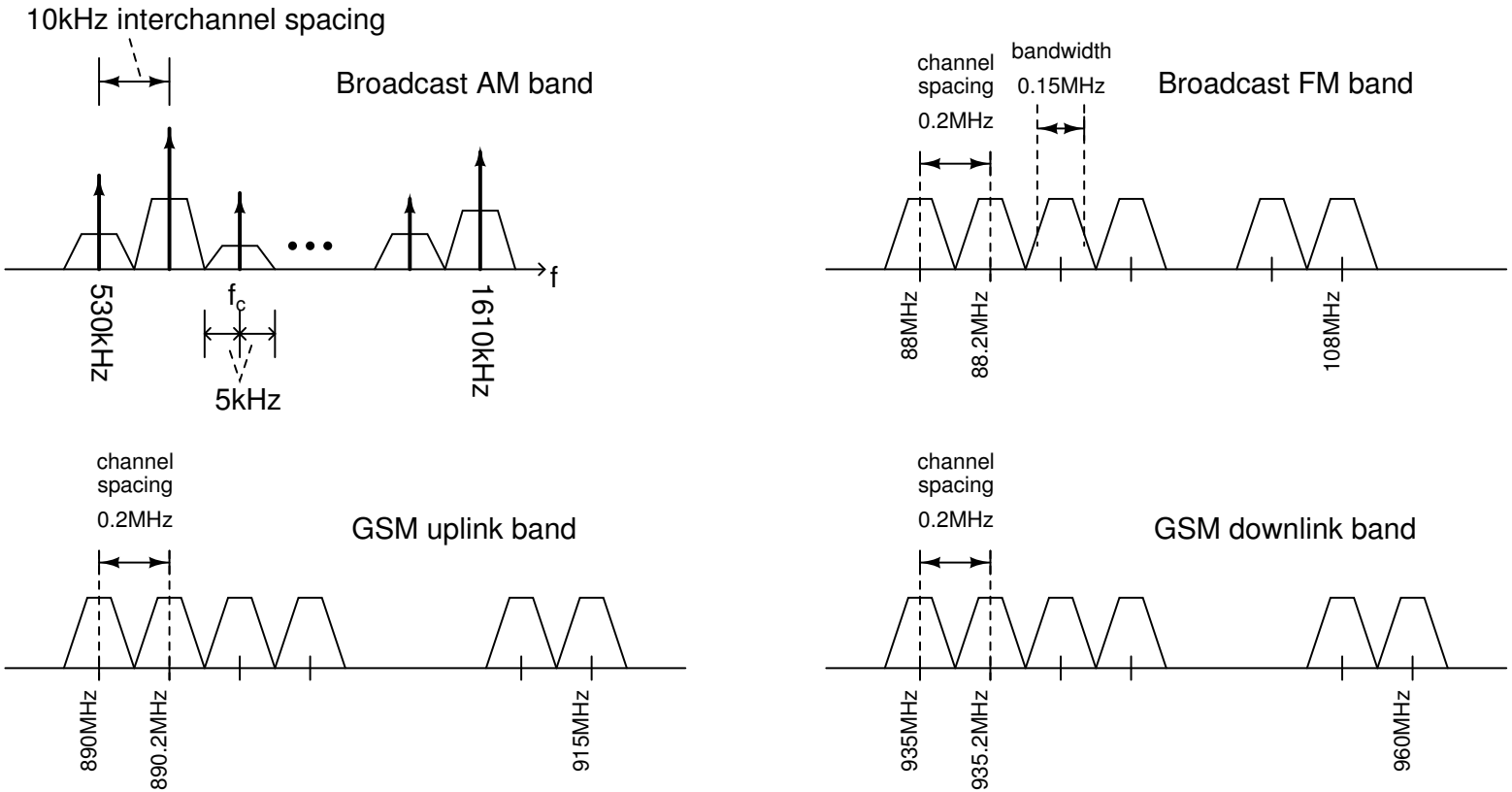
Outline

- Phase locked loop (PLL) requirements
- PLL frequency multiplier
  - Derivation
  - Phase model
- Type I PLL
  - Practical phase detectors
  - Type I PLL limitations
- Type II PLL
  - Feedback systems and stability
  - Type II PLL
- LC oscillator
- Programmable frequency divider

Phase locked loops

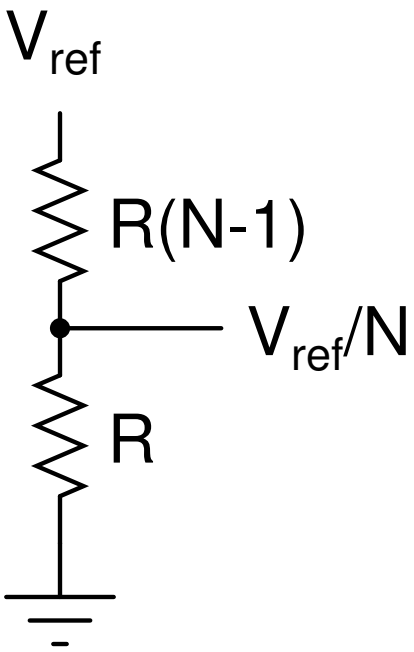
- Frequency synthesizers in radios for local oscillators
- Frequency multiplication for reference clock generation
- Phase alignment

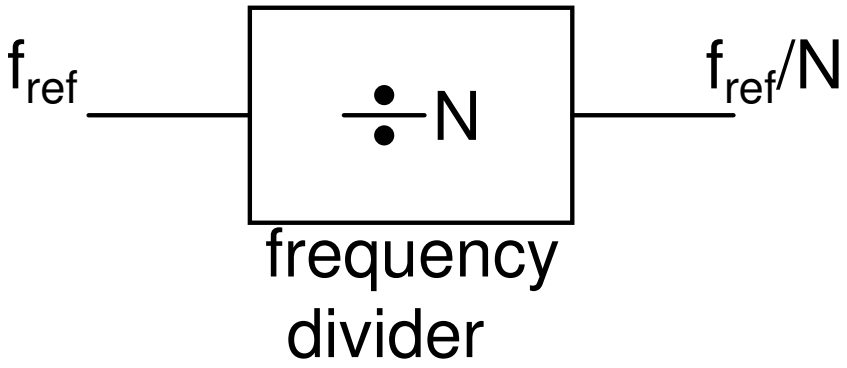
Local oscillator requirements



- Tuned to the desired channel frequency plus an intermediate frequency (IF)
- Generate equally spaced frequencies from a reference frequency
- Waveform shape not very important
- Spurious output and noise must be sufficiently low

Frequency divider



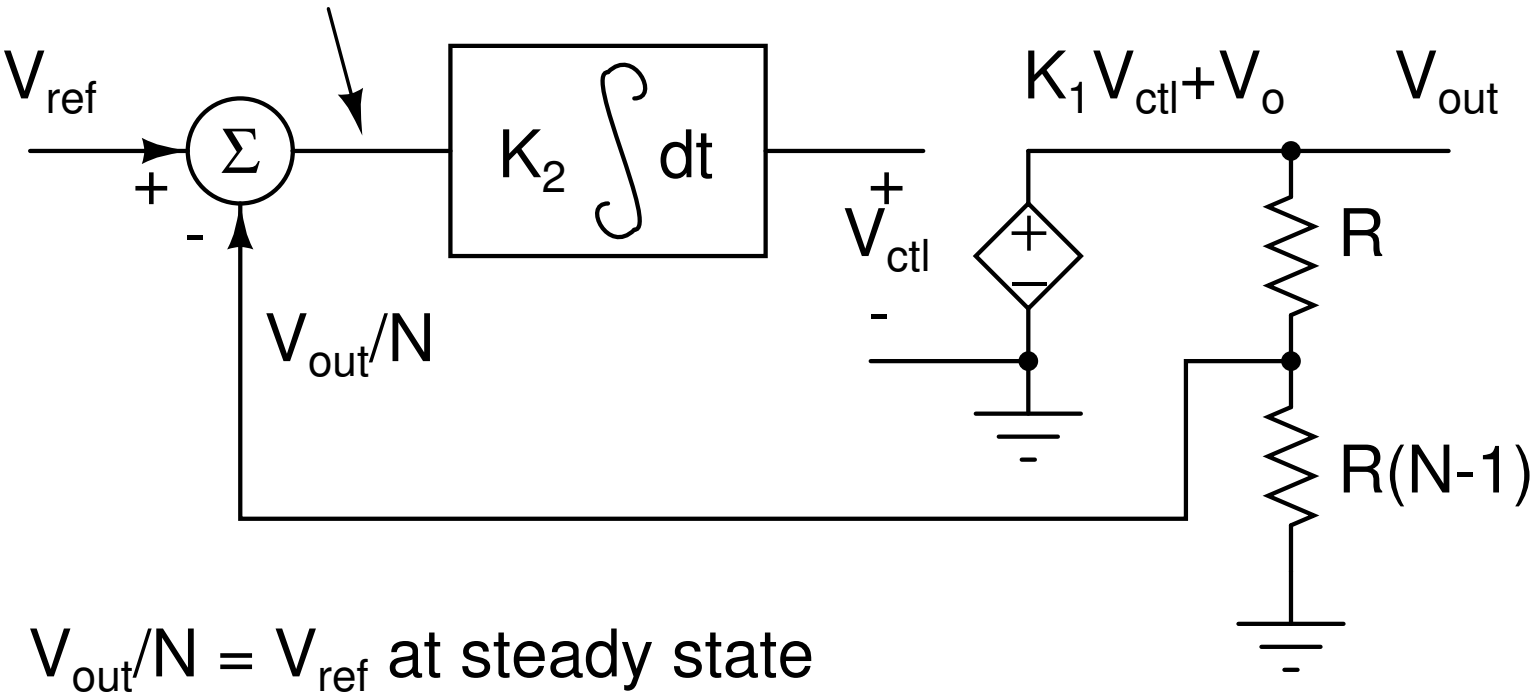


- Digital frequency divider can generate multiple frequencies
- Frequencies not equally spaced
- Reference frequency higher than output frequencies

Voltage multiplier

voltage difference

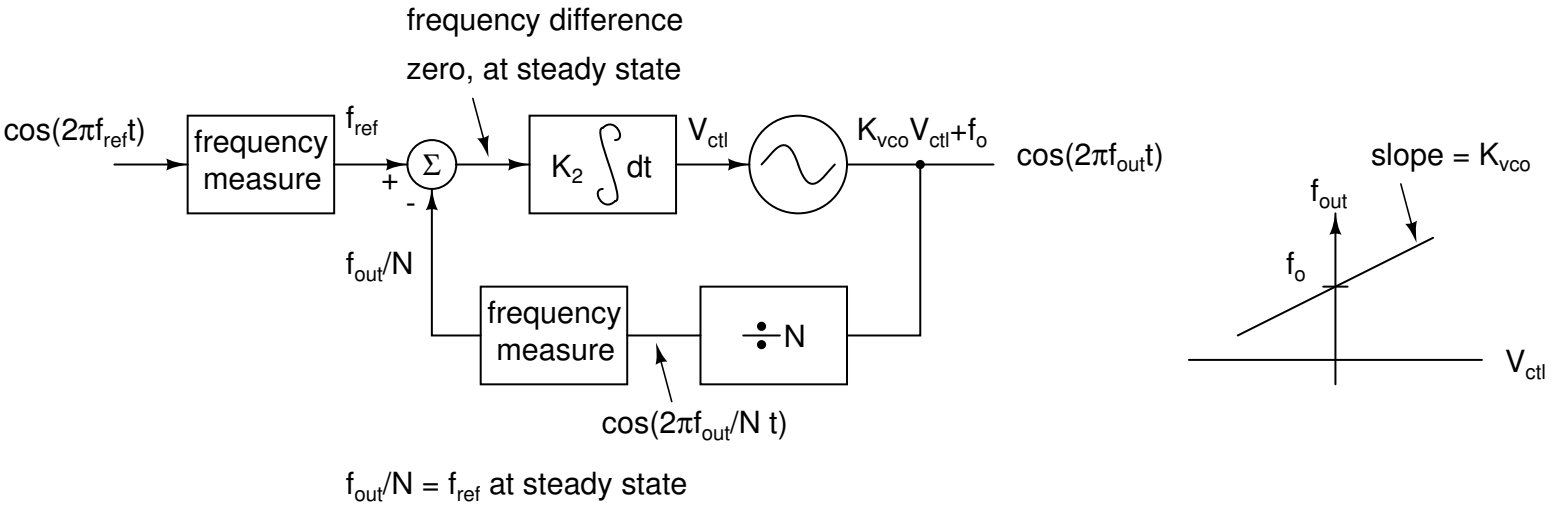
zero, at steady state



$V_{out}/N = V_{ref}$ at steady state

- A controlled source to generate the output voltage
- Divided output voltage subtracted from the reference to generate error
- Output source controlled by the integral of the error

Frequency multiplier

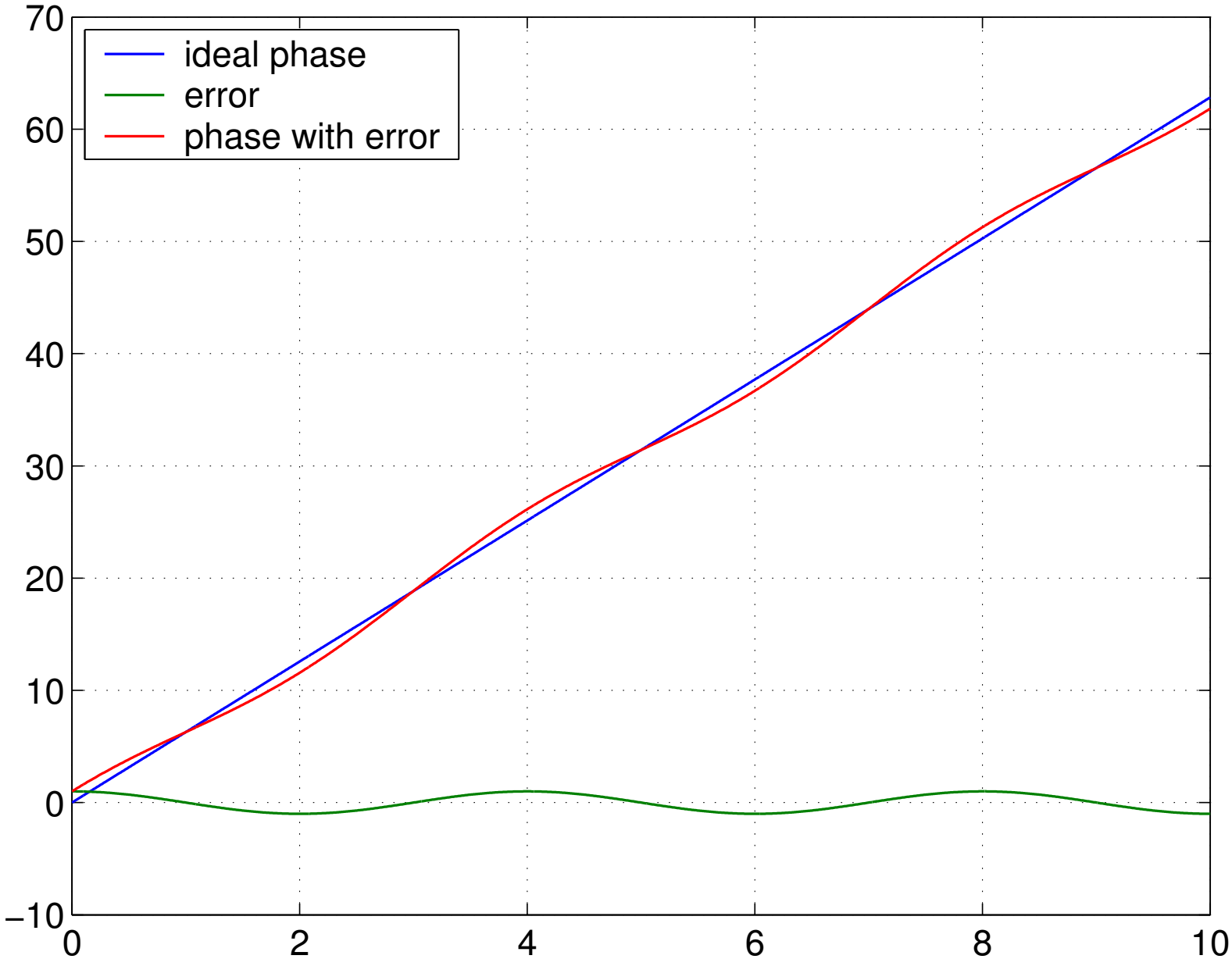


- A controlled source to generate the output frequency
  - A voltage controlled oscillator
- Divided output frequency subtracted from the reference frequency to generate error
- Output source controlled by the integral of the frequency error

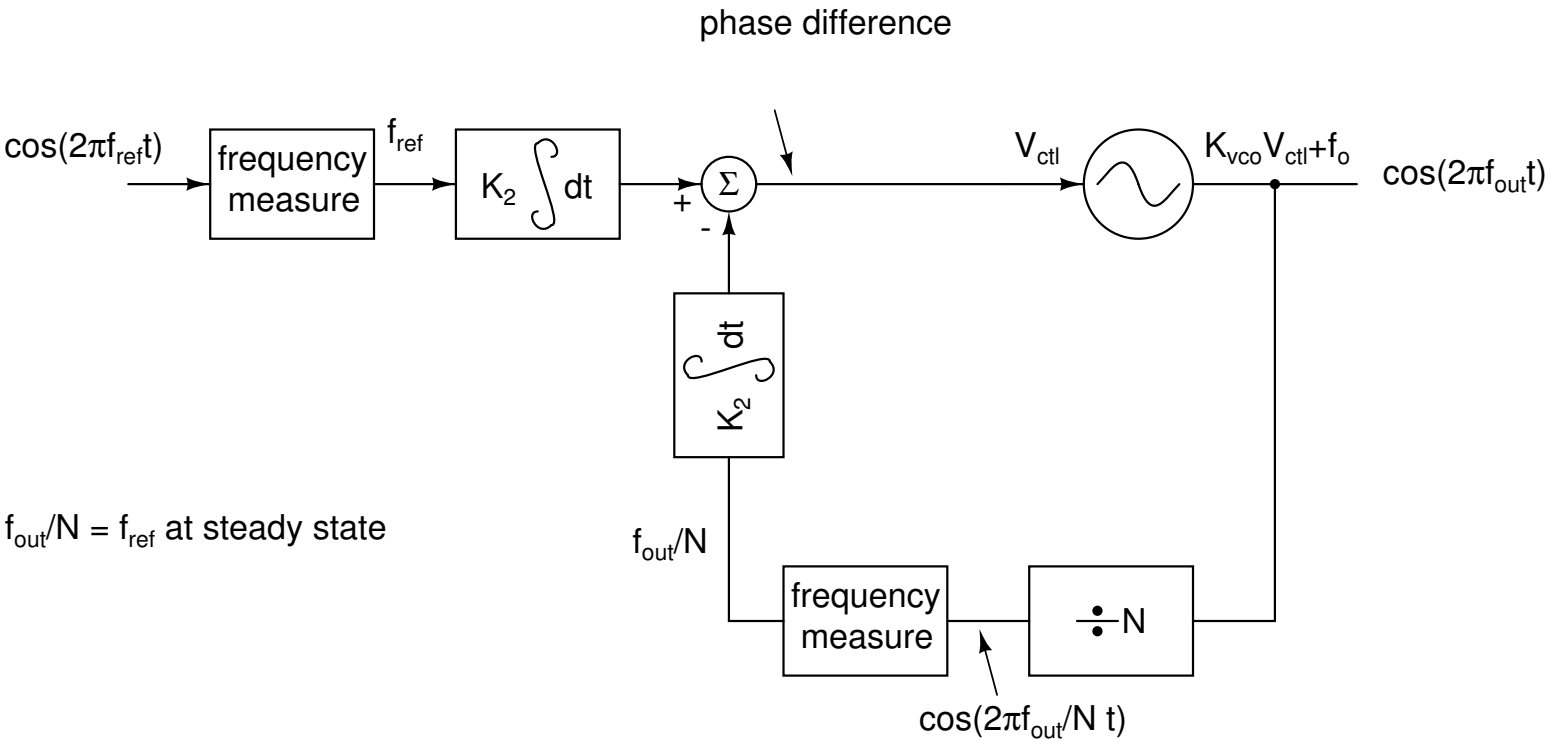
Phase and frequency

- Sinusoid: $\cos(\theta(t))$
- Phase: $\theta(t)$
- Instantaneous frequency: $f_i = \frac{1}{2\pi}\frac{d\theta(t)}{dt}$
- Typically expressed as $f_i = f_o + f_e(t)$
  - f_o: average frequency
  - f_e: instantaneous frequency error
- Phase $\theta(t) = 2\pi f_o t + \Phi_o + 2\pi \int f_e(t)dt$
- Phase $\theta(t) = 2\pi f_o t + \Phi_o + \phi(t)$
  - Φ_o: phase offset-ideal ramp versus time
  - $\phi(t)$: instantaneous phase

Phase error

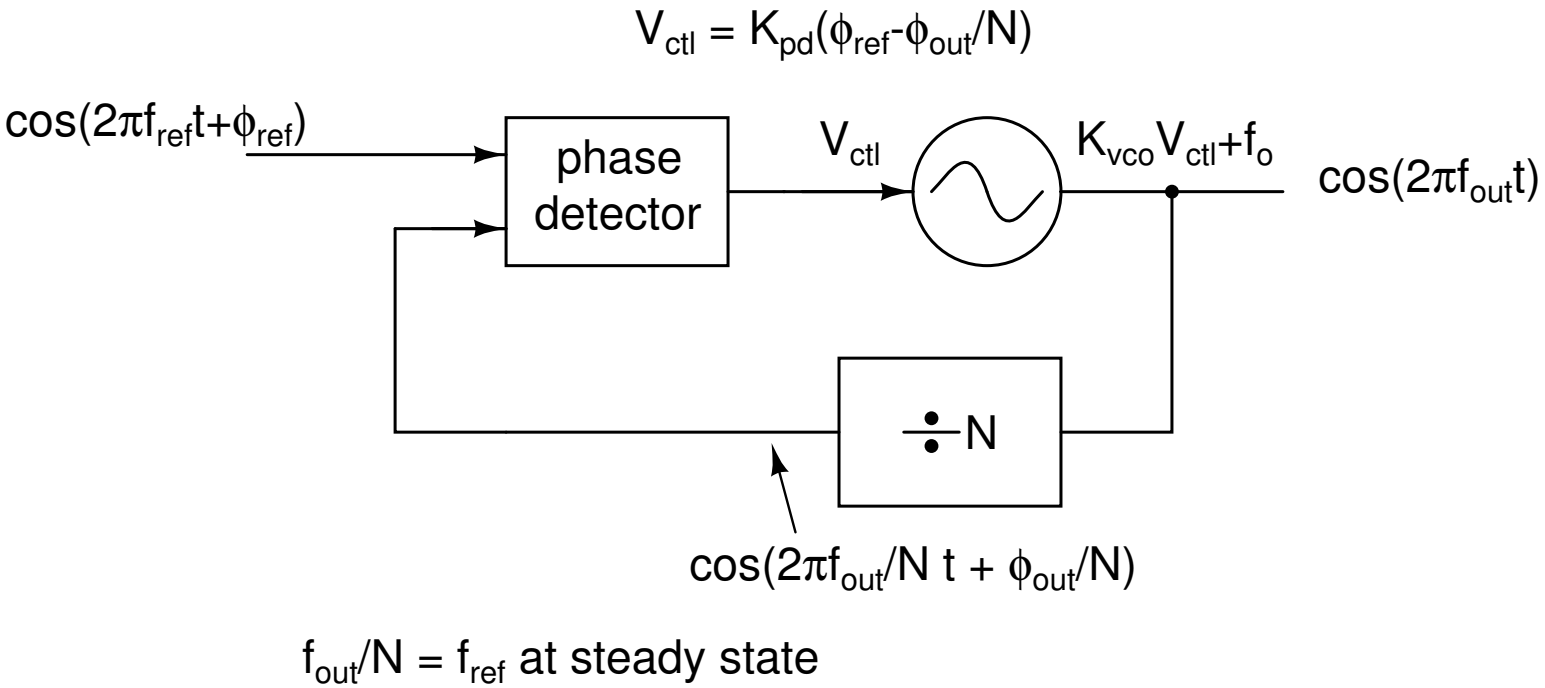

ideal phase
error
phase with error
70
60
50
40
30
20
10
0
−10
0
2
4
6
8
10

Frequency multiplier



- Integration before subtraction
- Integral of the frequency is phase
- Integrator+subtractor measures phase difference between the reference input and the divided output (feedback)

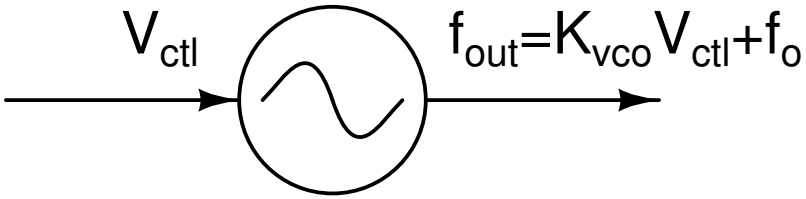
Frequency multiplier—Phase locked loop

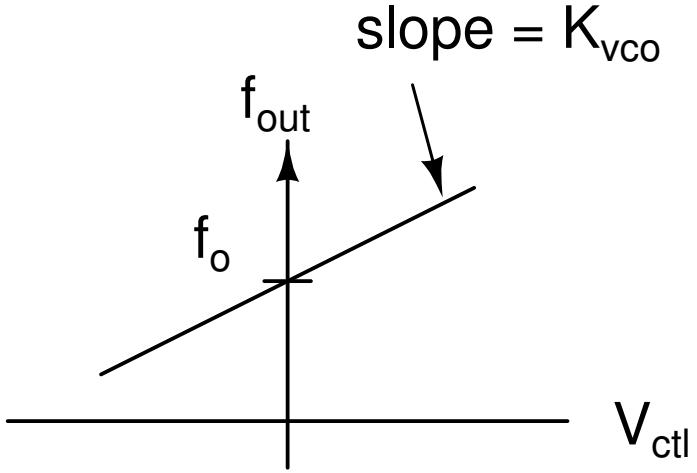


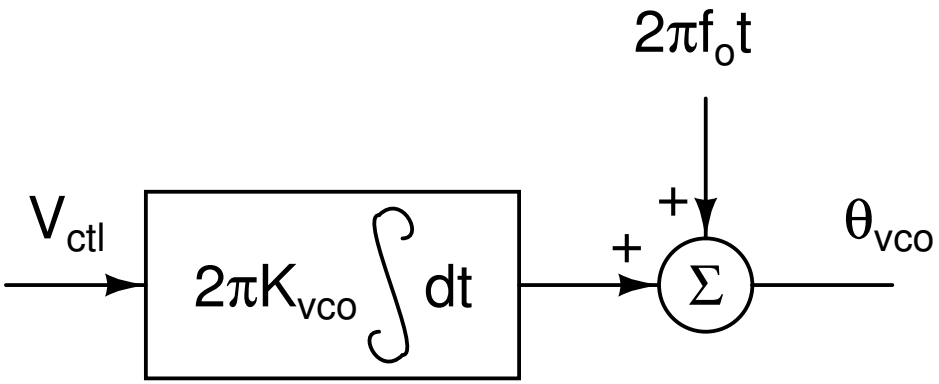
$f_{out}/N = f_{ref}$ at steady state

- Use a phase detector to generate the control voltage

Voltage controlled oscillator

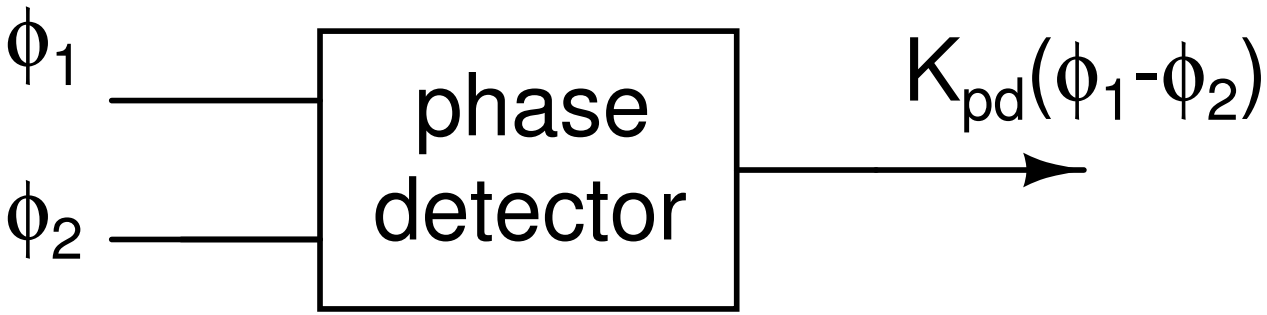






- $f_{vco} = f_o + K_{vco} V_{ctl}$
  - f_o: Free running frequency
- $\theta_{vco} = 2\pi f_o t + 2\pi K_{vco} \int V_{ctl} dt$
- K_{vco}: VCO gain in Hz/V

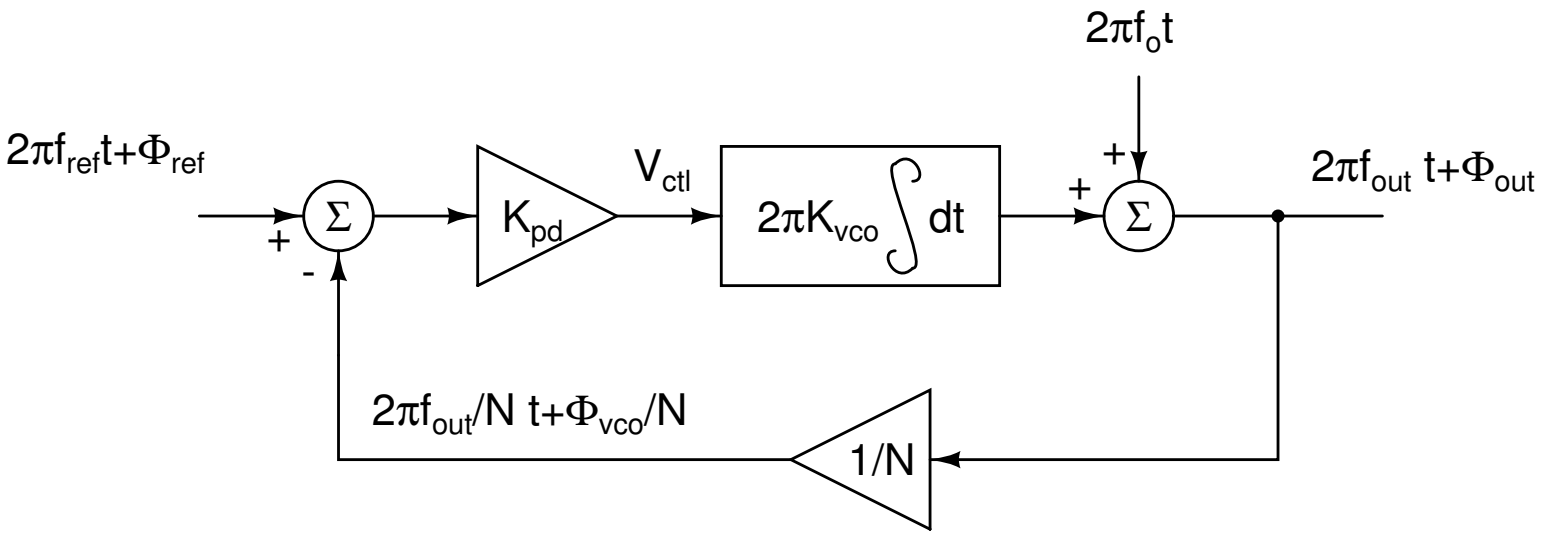
Phase detector



K_{pd}: phase detector gain

- K_{pd}: Phase detector gain in V/radian
- Ideal phase detector: assumed to have an output $V_{pd} = K_{pd}(\phi_1 - \phi_2)$

Phase locked loop model

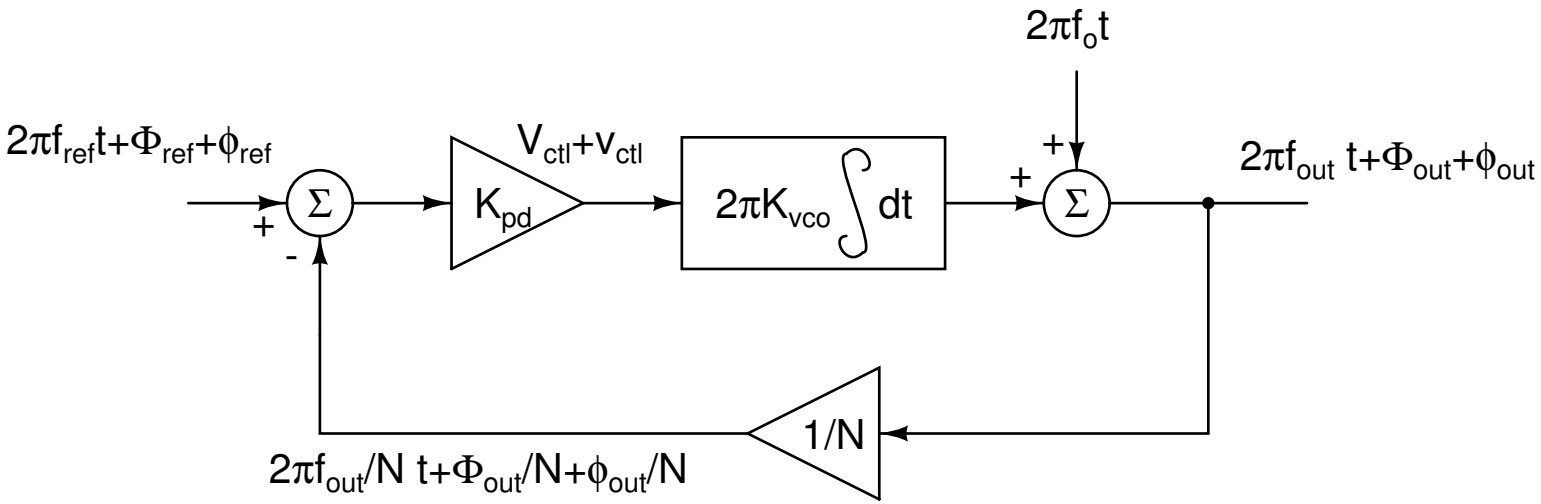


$V_{ctl} = 2\pi(f_{ref}-f_{out}/N)t + \Phi_{ref} - \Phi_{out}/N$

At steady state, $f_{ref}=f_{out}/N$; $V_{ctl} = \Phi_{ref} - \Phi_{out}/N$

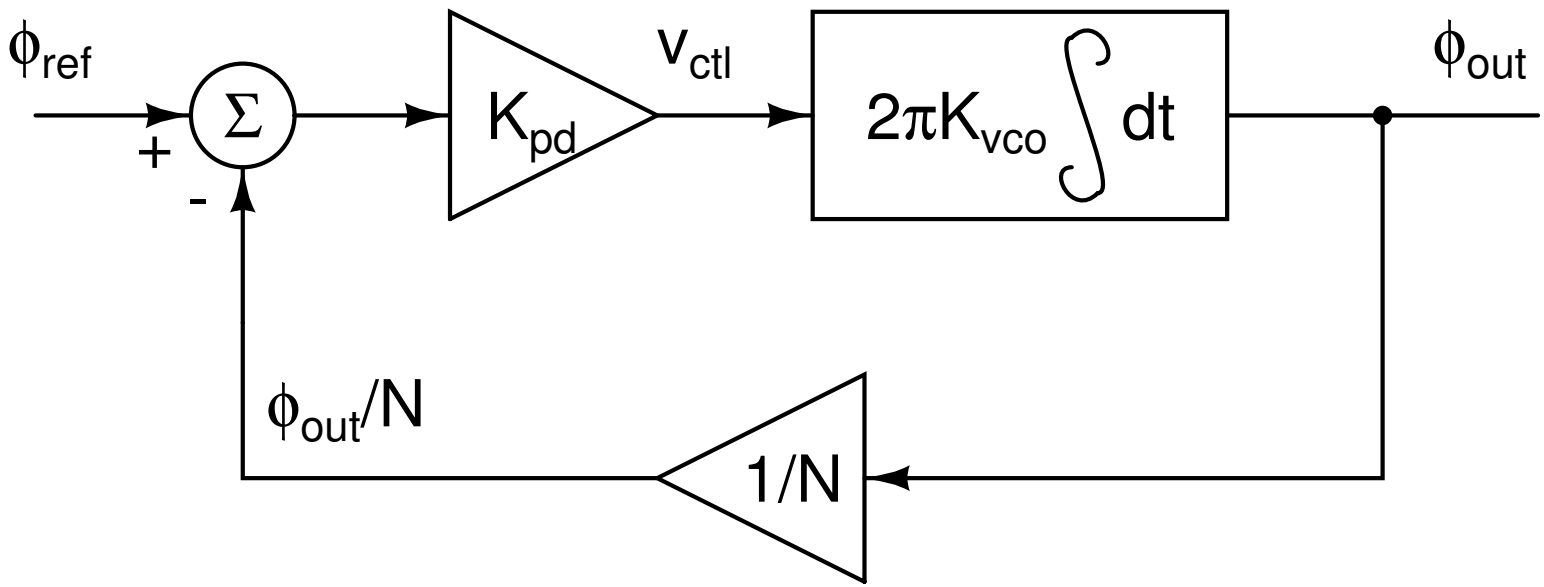
- Modelled in terms of phases of signals
- At steady state (lock), V_{ctl} is a constant $\Rightarrow f_{ref} = f_{out}/N$
- The loop locks with $V_{ctl} = K_{pd}(\Phi_{ref} - \Phi_{out}/N) = (Nf_{ref} - f_o)/K_{vco}$—This is the "operating point" of the circuit

Phase locked loop model



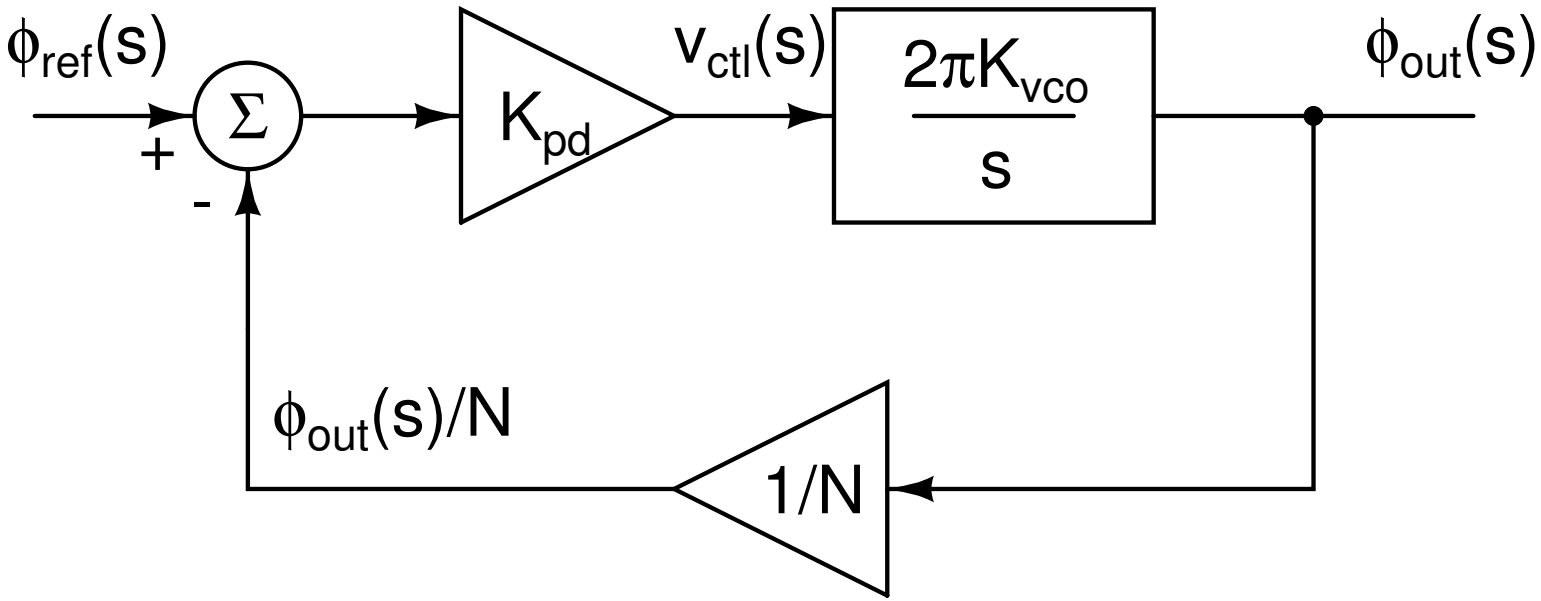
- An increment ϕ_{ref} in the input phase causes increments ϕ_{out}, v_{ctl}

Phase locked loop model—incremental picture



- An increment ϕ_{ref} in the input phase causes increments ϕ_{out}, v_{ctl}
- Type-I loop—One integrator in the loop
- "Phase model" of the PLL

Phase locked loop model—frequency domain



- Loop gain $L(s) = 2\pi K_{pd} K_{vco}/Ns$
- Transfer function
  $\phi_{out}(s)/\phi_{ref}(s) = N/(1 + Ns/(2\pi K_{pd} K_{vco}))$
- Type-I loop—One integrator in the loop
- Closed loop bandwidth (= unity loop gain frequency)
  $= 2\pi K_{pd} K vco/N$ rad/s

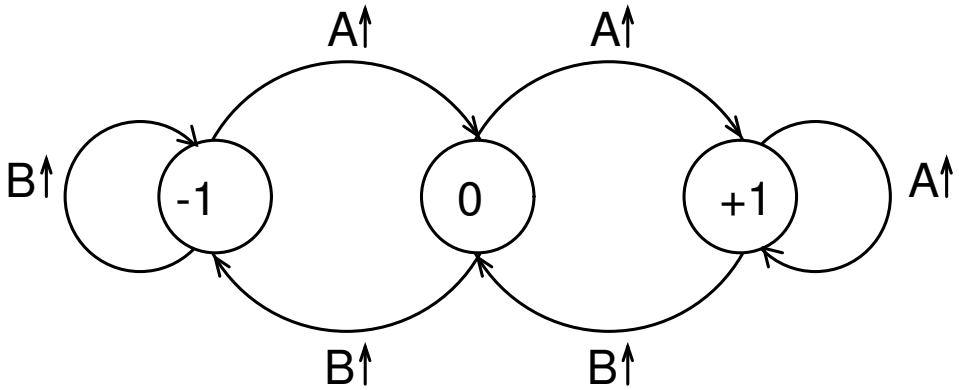
Type-I PLL—limitations

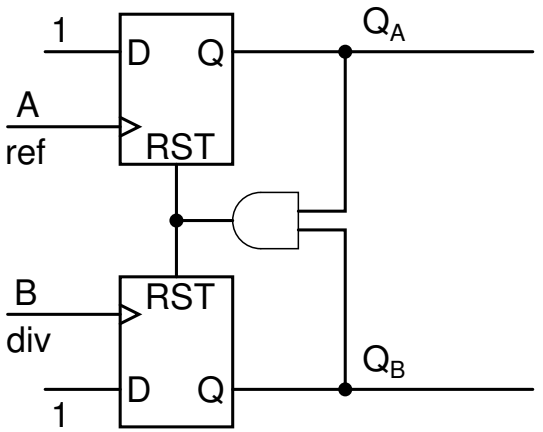
- Phase error when locked ($f_{out} = Nf_{ref}$):
  - $\Phi_{ref} - \Phi_{out}/N = (Nf_{ref} - f_o)/K_{vco}K_{pd}$
  - dc value of K_{pd} matters; We have a constant K_{pd}
- $|\Phi_{ref} - \Phi_{out}/N| < 2\pi \Rightarrow |f_{out} - f_o| < 2\pi K_{pd}K_{vco}$
- Lock range limited by periodicity of phase detector
  - Period of all phase detectors not necessarily $\pm 2\pi$
  - Commonly used three state phase detector periodic with $\pm 2\pi$
- $K_{pd}K_{vco}$ large for wide lock range

Phase detector

- Frequency divider output has a varying duty cycle
- Phase detector should sensitive to duty cycle
  - XOR gate etc. are not preferable
- Phase detector should be sensitive *only* to rising edges (or *only* to falling edges) of inputs

Tri state phase detector

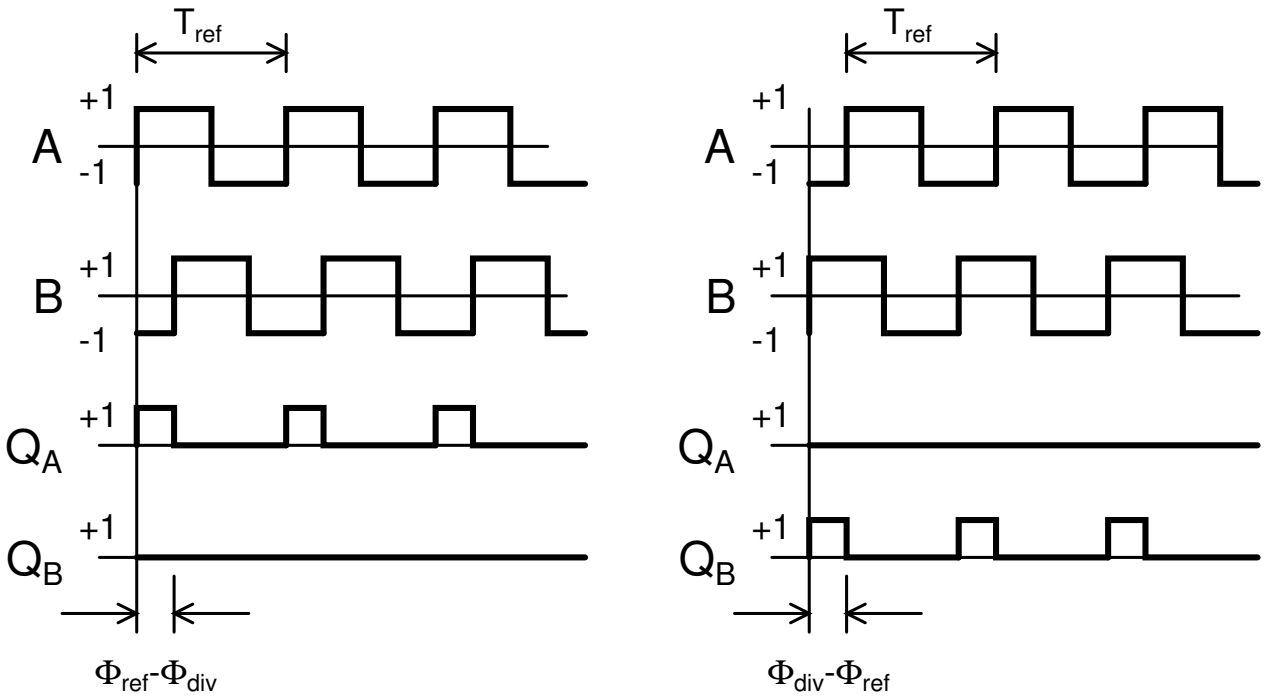




output=Q_A-Q_B

- Output $+1, -1, 0$
  - $+1$ if reference leads divider output
  - -1 if reference lags divider output
  - 0 if reference coincides with divider output

Tri state phase detector-waveforms

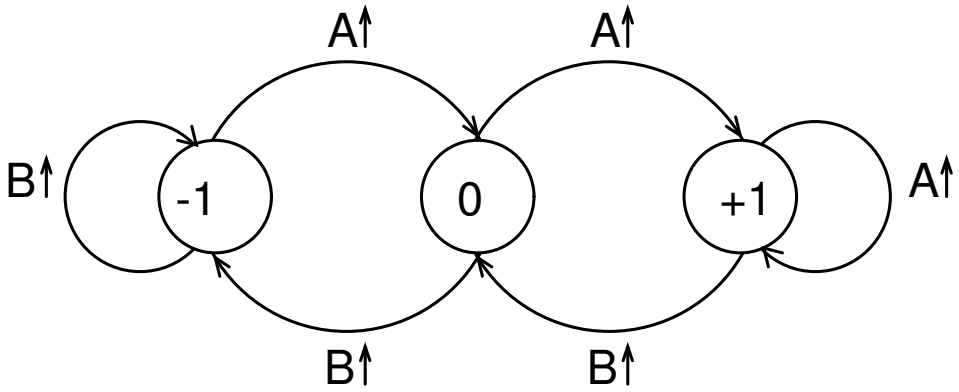


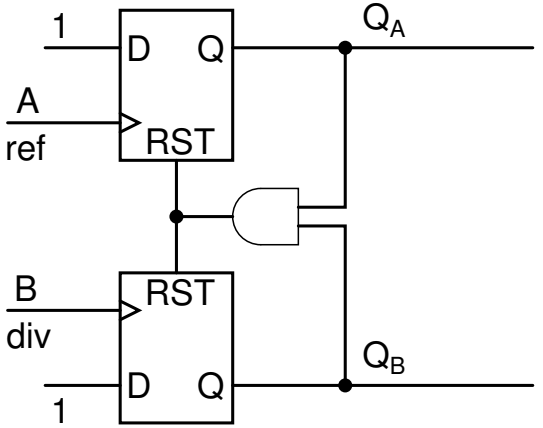
A leading B

A lagging B

- Flip flops assumed to be reset instantaneously

Tri state phase detector-frequency difference between inputs



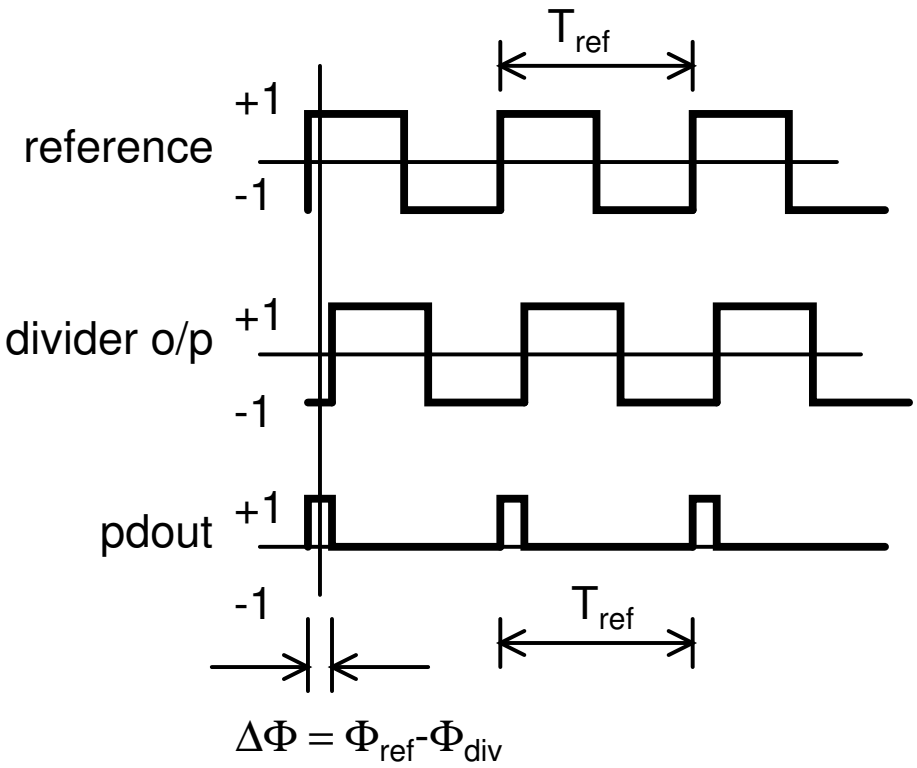


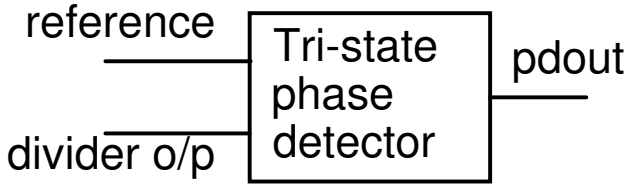
output=Q_A-Q_B

- $f_A > f_B$: Eventually get two consecutive edges of A
- Circulates between 0 and $+1$ states: Average output > 0
- Similarly, average output > 0 for $f_A < f_B$

This detector is a phase/frequency detector (PFD)

Tri state phase detector output





Average value = $\Delta\Phi/\pi$

Output periodic at f_{ref}

$$V_{out}(f) = \frac{\Delta\Phi}{2\pi} \sum_{n=-\infty}^{\infty} \text{sinc}\left(\frac{n\Delta\Phi}{2\pi}\right) \delta(f - nf_{ref})$$

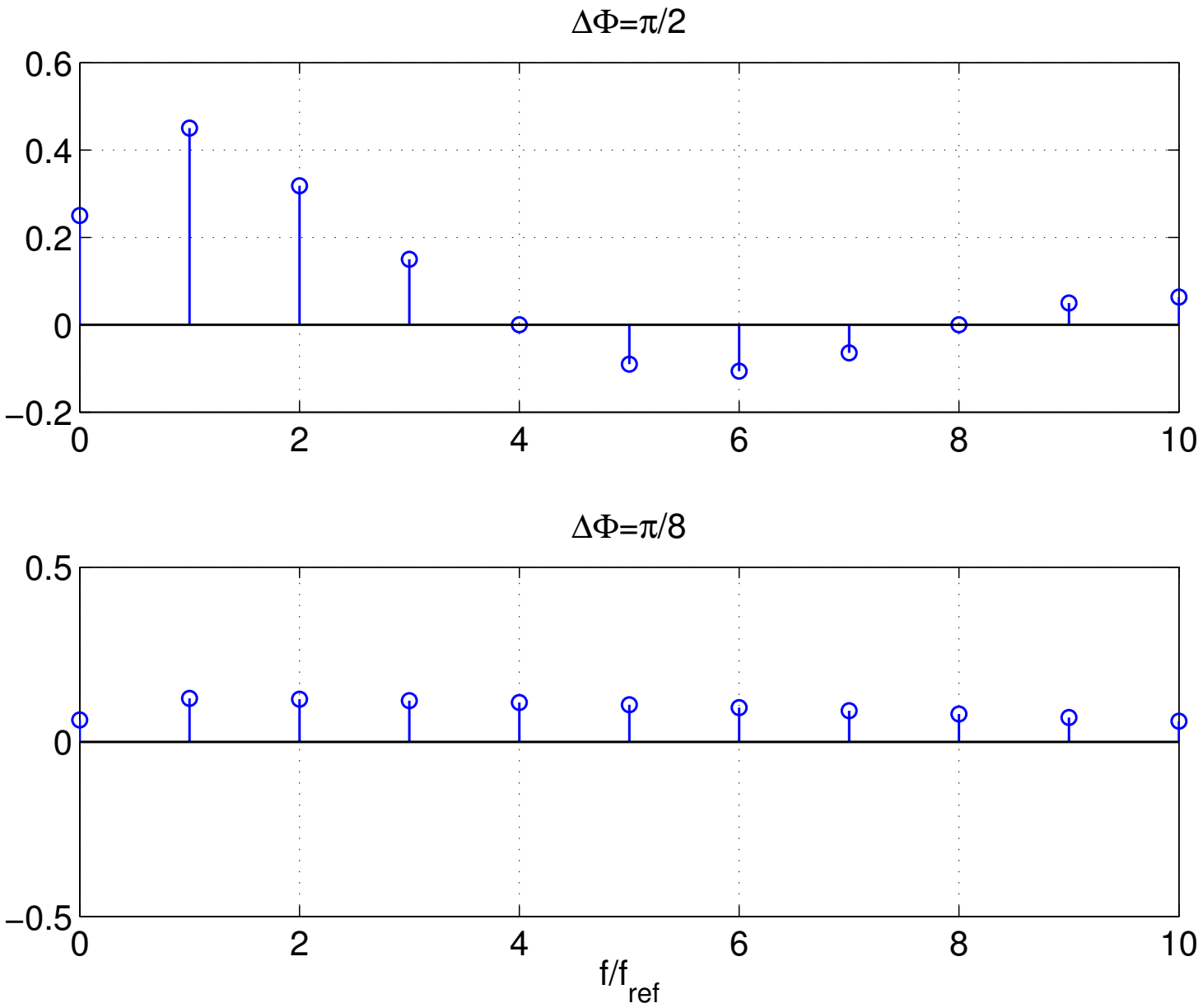
$$V_{out}(t) = \frac{\Delta\Phi}{2\pi} + \frac{\Delta\Phi}{\pi} \sum_{n=1}^{\infty} \text{sinc}\left(\frac{n\Delta\Phi}{2\pi}\right) \cos(2\pi nf_{ref}t)$$

Tri state phase detector

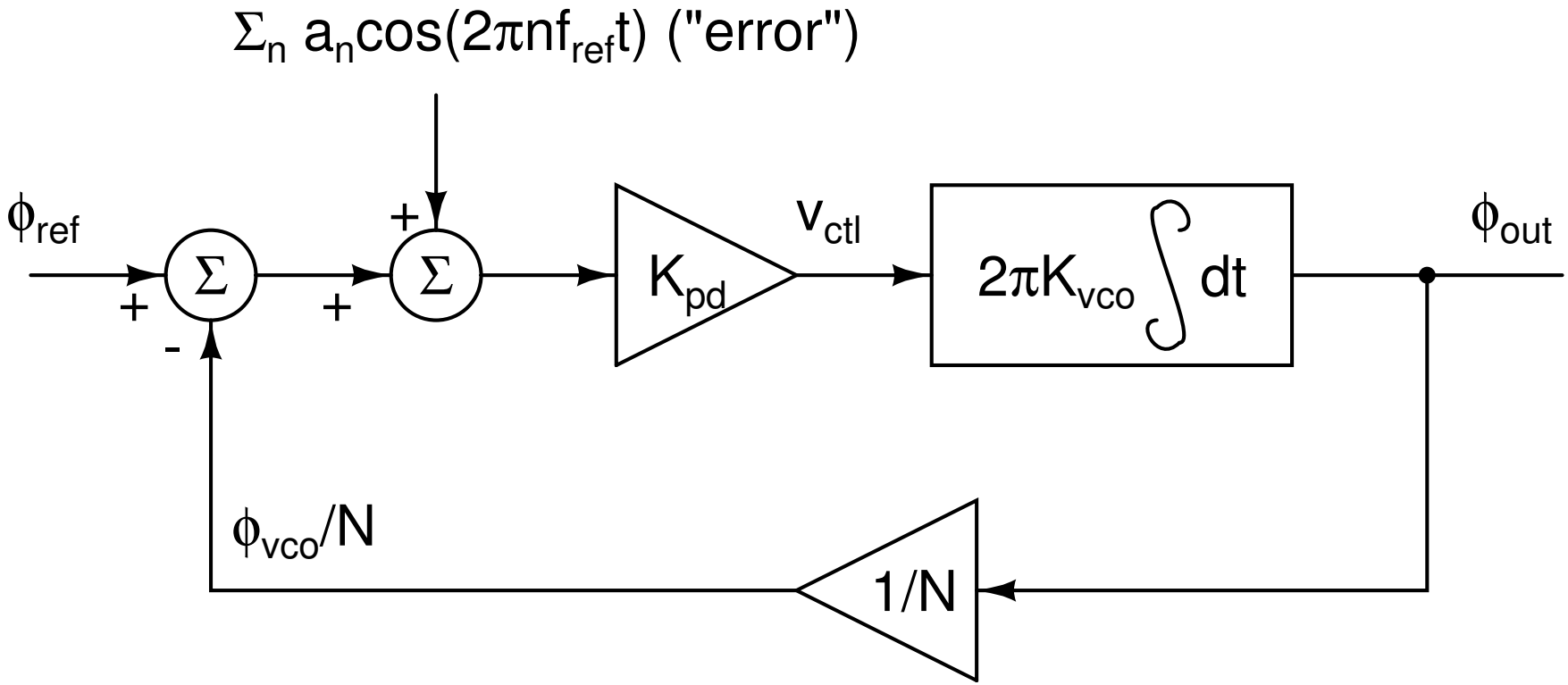
- Output average value = $\Delta\Phi/2\pi$
  - $K_{pd} = 1/2\pi$
  - Phase detector offset $= 0$
  - Loop locks with $\Delta\Phi = \Phi_{ref} - \Phi_{out}/N = 0$ for $Nf_{ref} = f_o$
  - Input range = $\pm 2\pi$
  - PLL lock range = $f_o - 2\pi K_{pd} K_{vco} < f_{out} < f_o + 2\pi K_{pd} K_{vco}$
- Output contains f_{ref} and its harmonics
- Output = $1/2\pi\,(\Delta\Phi + \sum_n a_n \cos(2\pi n f_{ref} t))$
- Periodic signal in addition to $K_{pd}\Delta\Phi$

All real phase detectors have a periodic “error” in addition to the “dc” term proportional to phase error

Phase detector-Output spectrum

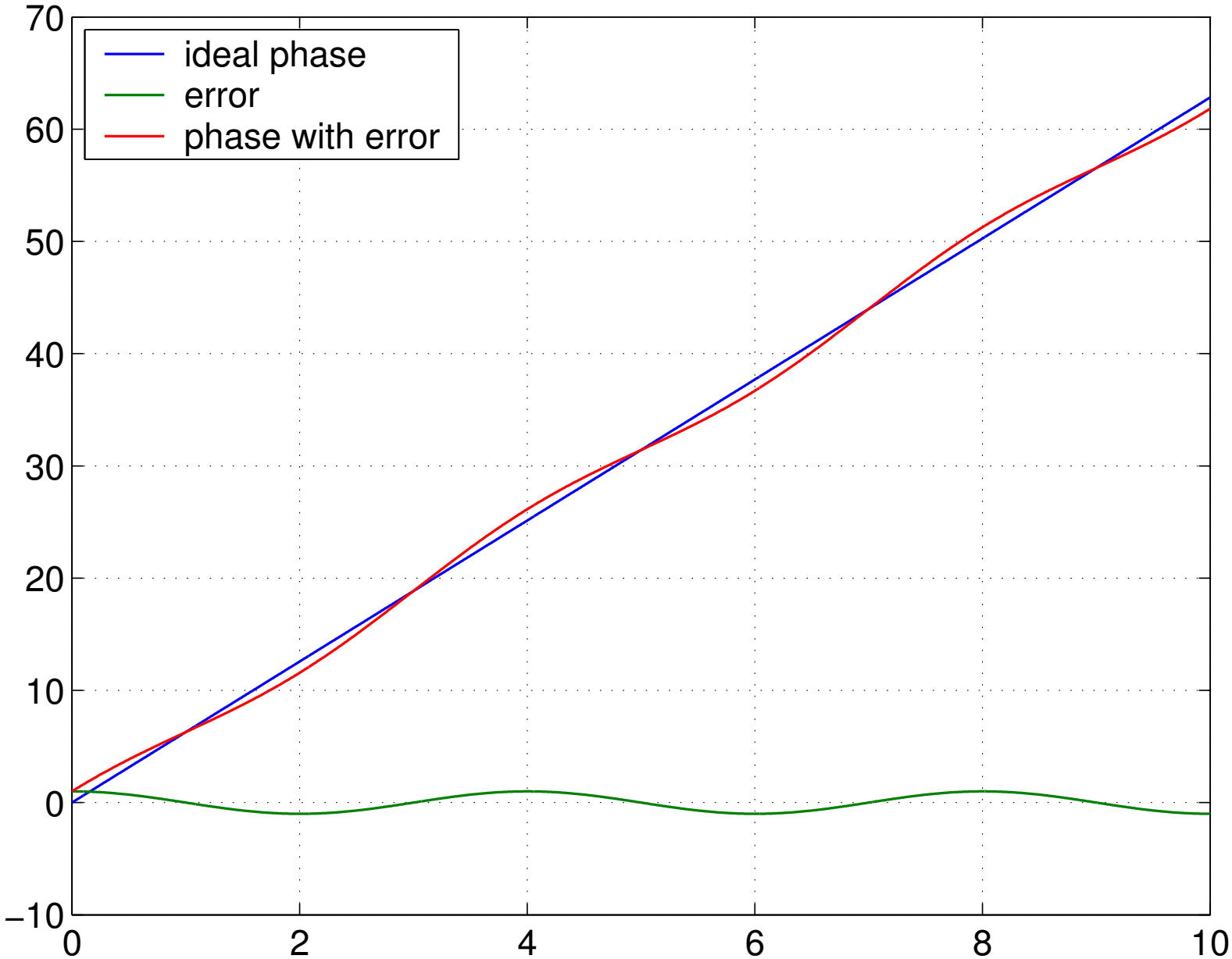


PLL with tri state phase detector—periodic error

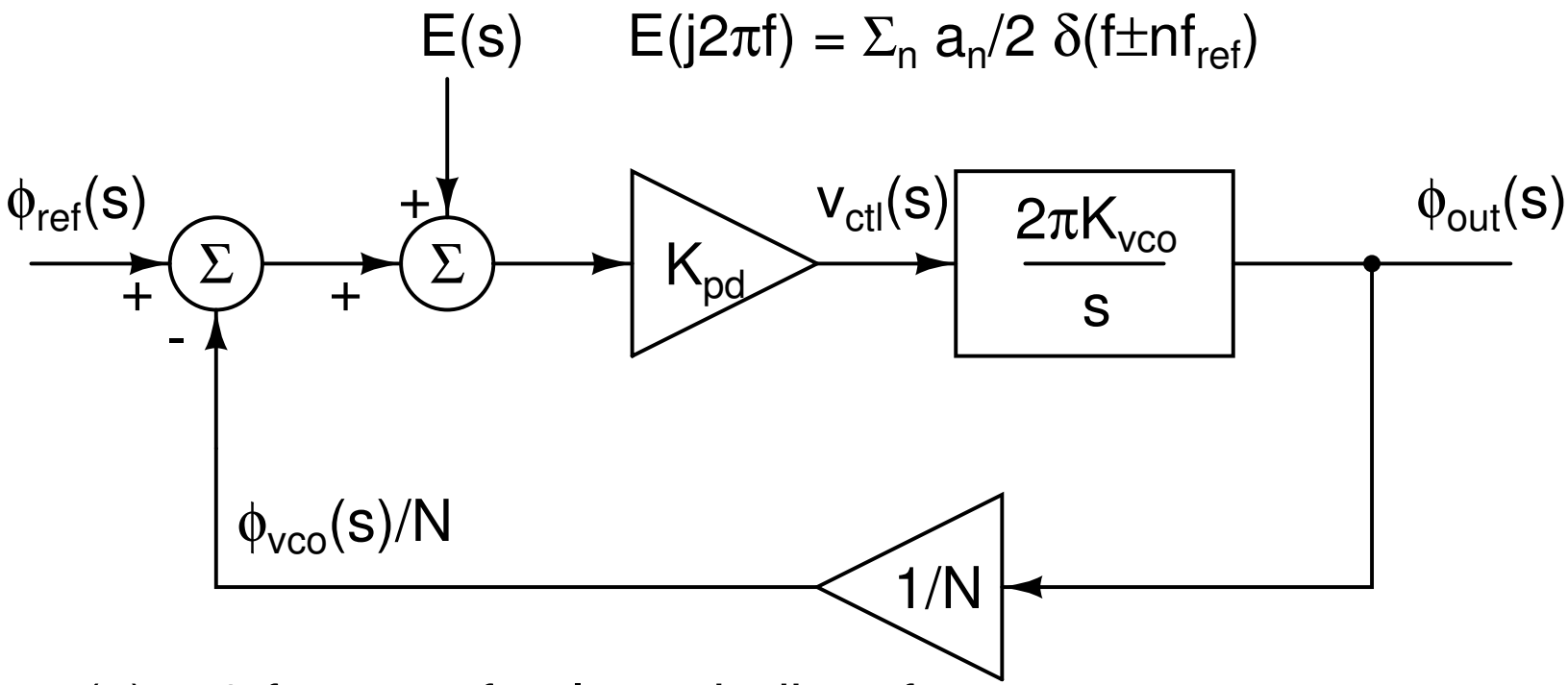


- Error $e(t)$ added to the input of the phase detector
- Disturbances in the VCO output phase $\phi_{out}(t)$ even with a perfect reference ($\phi_{ref}(t) = 0$)
- VCO output: $\cos(2\pi N f_{ref} t + N\Phi_{ref} + \phi_{out}(t))$
- VCO output not periodic at $N f_{ref}$

Phase error


ideal phase
error
phase with error
70
60
50
40
30
20
10
0
−10
0
2
4
6
8
10

PLL with tri-state phase detector—frequency domain



$\phi_{ref}(s) = 0$ for a perfectly periodic reference

- Transfer function from the error to the output
  $\phi_{out}(s)/E(s) = \phi_{out}(s)/\phi_{ref}(s) = N/(1 + Ns/(2\pi K_{pd}K_{vco}))$
- $E(j2\pi f) = \sum_n (a_n/2)\delta(f \pm nf_{ref})$

Type-I PLL

$$\begin{aligned}\frac{\phi_{out}(s)}{E(s)} &= \frac{\phi_{out}(s)}{\phi_{ref}(s)} \\ &= N\frac{2\pi K_{pd}K_{vco}/Ns}{1+2\pi K_{pd}K_{vco}/Ns} \\ &= N\frac{1}{1+sN/2\pi K_{pd}K_{vco}}\end{aligned}$$

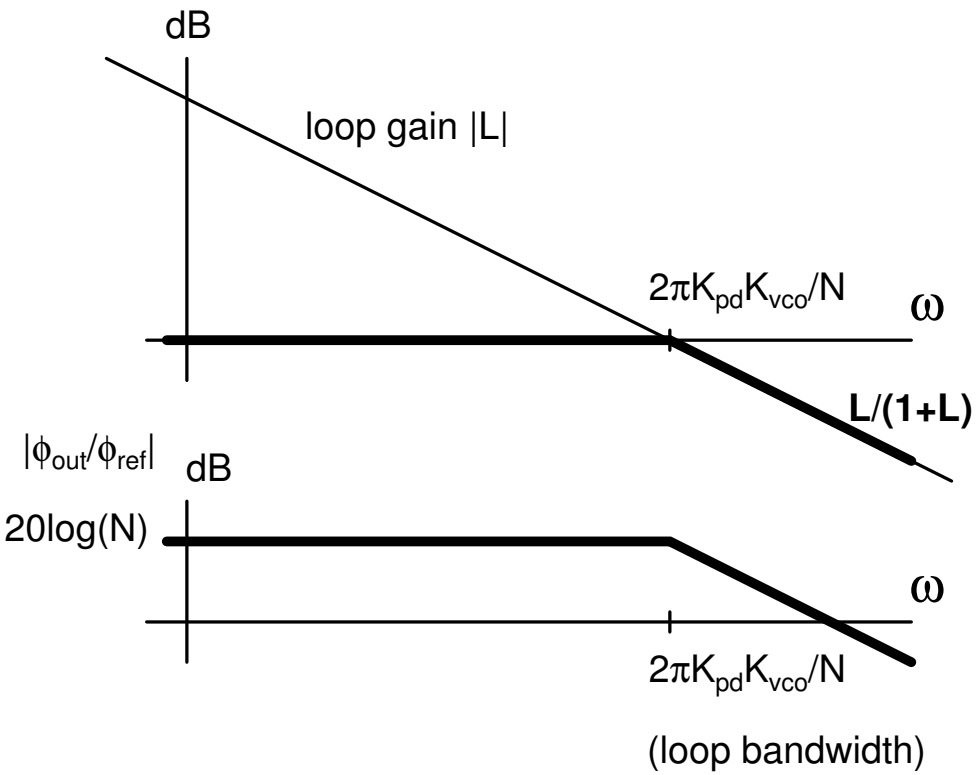
Loop gain

$$L(s) = \frac{2\pi K_{pd}K_{vco}}{Ns}$$

Closed loop bandwidth (Hz)

$$f_{-3dB} = \frac{K_{pd}K_{vco}}{N}$$

Type I PLL


dB
loop gain |L|
$2\pi K_{pd}K_{vco}/N$
ω
L/(1+L)
$|\phi_{out}/\phi_{ref}|$
dB
20log(N)
ω
$2\pi K_{pd}K_{vco}/N$
(loop bandwidth)

Feedback system

In our system,

$$\frac{\phi_{out}(s)}{E(s)} = N\frac{2\pi K_{pd}K_{vco}/Ns}{1+2\pi K_{pd}K_{vco}/Ns}$$

In general, in a feedback system with a loop gain $L(s)$

$$H_{closedloop}(s) = H_{ideal}(s)\frac{L(s)}{1+L(s)}$$

Where $H_{ideal}(s)$ is the ideal closed loop gain (with $L=\infty$). This can be approximated as

$$\begin{aligned} H_{closedloop}(s) &= H_{ideal}(s)L(s) && |L| \ll 1 \\ &= H_{ideal}(s) && |L| \gg 1 \end{aligned}$$

PLL with tri state phase detector—Output signal

Considering only the term at f_{ref}, and $b_1 \ll 1$

$$\begin{aligned} V_{out}(t) &= \cos(2\pi N f_{ref} t + b_1 \sin(2\pi f_{ref} t)) \\ &= \cos(2\pi N f_{ref} t)\cos(b_1 \sin(2\pi f_{ref} t)) \\ &\quad - \sin(2\pi N f_{ref} t)\sin(b_1 \sin(2\pi f_{ref} t)) \\ &\approx \cos(2\pi N f_{ref} t) - b_1 \sin(2\pi f_{ref} t)\sin(2\pi N f_{ref} t) \\ &= \cos(2\pi N f_{ref} t) \\ &\quad - b_1/2 \cos(2\pi(N-1) f_{ref} t) \\ &\quad - b_1/2 \cos(2\pi(N+1) f_{ref} t) \end{aligned}$$

- Spurious tones in the output at a spacing of $\pm f_{ref}$ from the desired frequency—"Reference feedthrough"
- In general, spurious tones will be present at $\pm n f_{ref}$ from the desired PLL output

Reference feedthrough

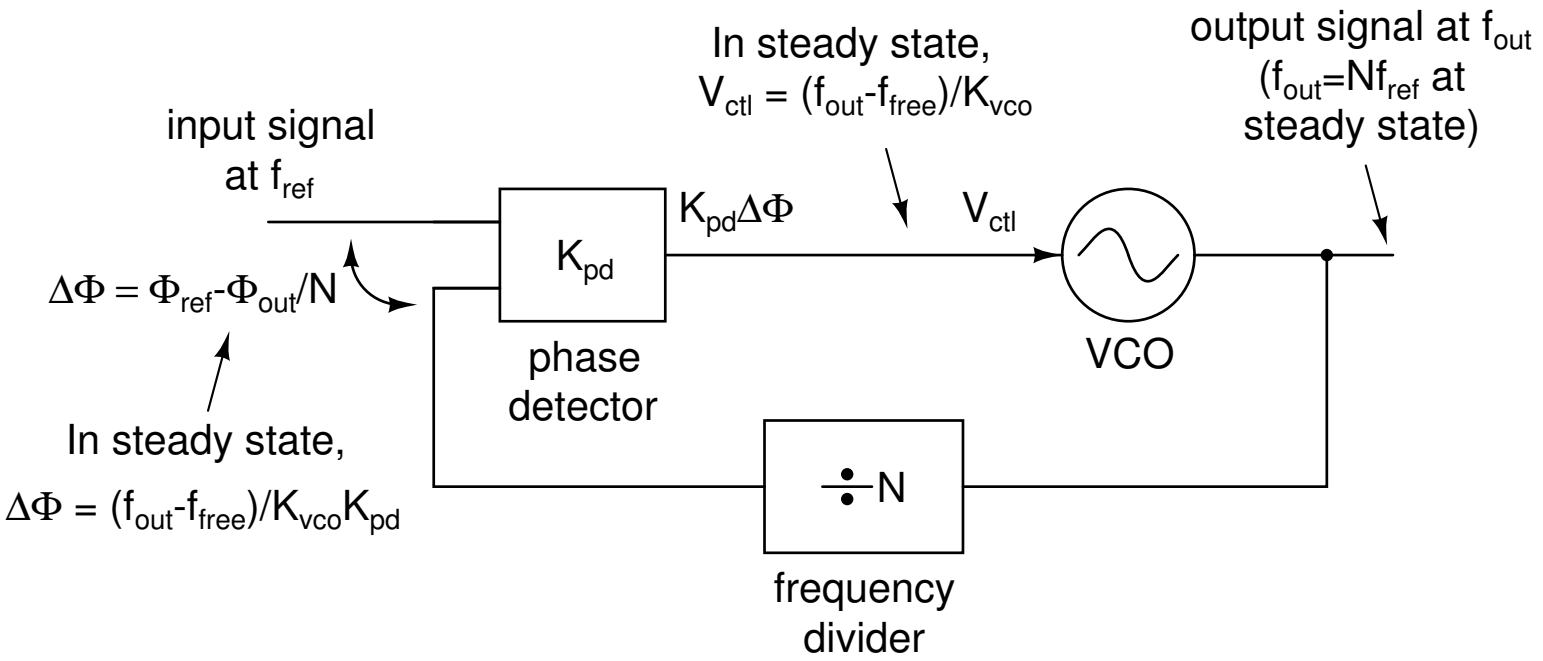
$$
\begin{aligned}
b_1 &= a_1 |H(j2\pi f_{ref})| \\
&= a_1 N \left| \frac{K_{pd} K_{vco}/jNf_{ref}}{1 + K_{pd} K_{vco}/jNf_{ref}} \right| \\
&\approx a_1 N \left| \frac{K_{pd} K_{vco}}{jNf_{ref}} \right| \\
&= 2\Delta\Phi \frac{Nf_{-3dB}}{f_{ref}} \operatorname{sinc} \frac{\Delta\Phi}{2\pi}
\end{aligned}
$$

- Maximum value of $b_1 = 4K_{pd}K_{vco}$ when $\Delta\Phi = \pi$

Reference feedthrough—example

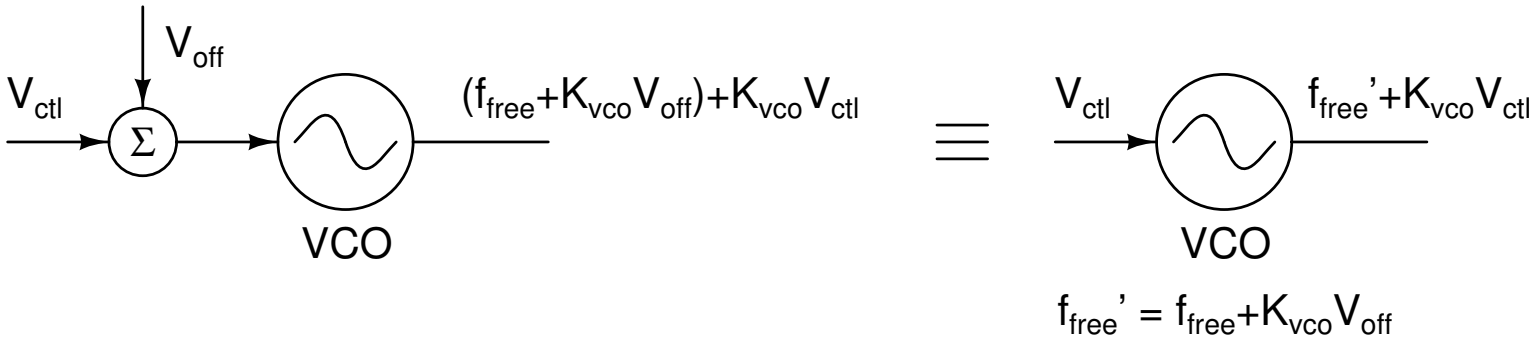
- To generate 1 GHz from 1 MHz reference
  - $b_1/2 = 10^{-2}$ (spurious tones at $(N \pm 1)f_{ref}$ 40 dB below the fundamental output at Nf_{ref})
  - $N = 10^3$
  - $\Delta\phi = \pi$ (locked with a phase shift of π)
- $f_{-3dB}/f_{ref} = 5 \times 10^{-6} \Rightarrow f_{-3dB} = 5\,\text{Hz}$
- Lock range $= 2\pi N f_{-3dB} \approx 10\pi\,\text{kHz}$
- Lock range is too small; Can't switch to the next channel which is 1 MHz away!
- May not be able to lock for any value of N, unless the free running frequency happens to be Nf_{ref} for some N

Type I phase locked loop



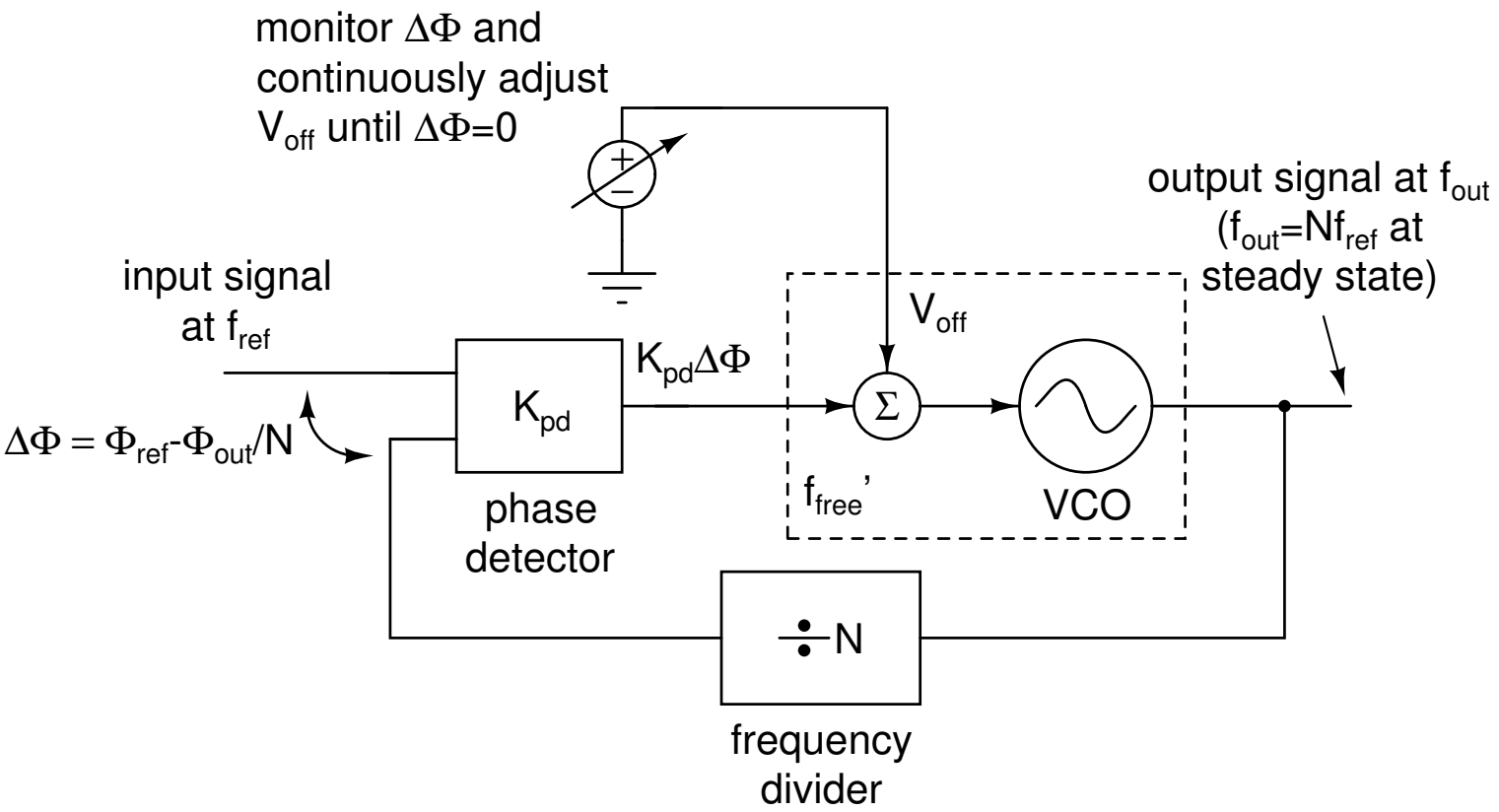
$\Delta\Phi = 0$ if f_{out} happens to be equal to f_{ref}. Zero spurs!

Changing the free running frequency of a VCO



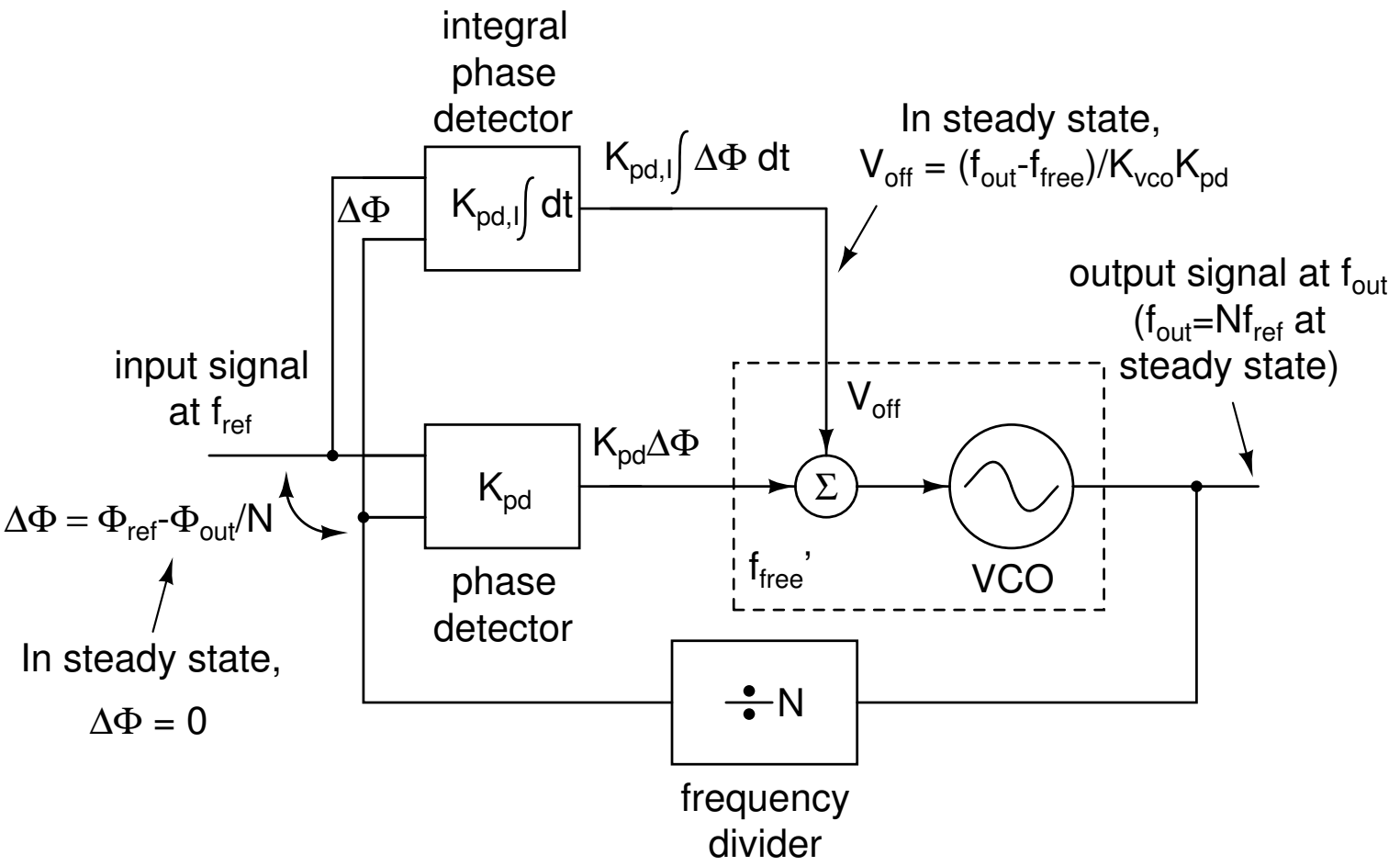
- Add a bias to the input to change the free running frequency

Slowly change the bias until $\Delta\phi = 0$



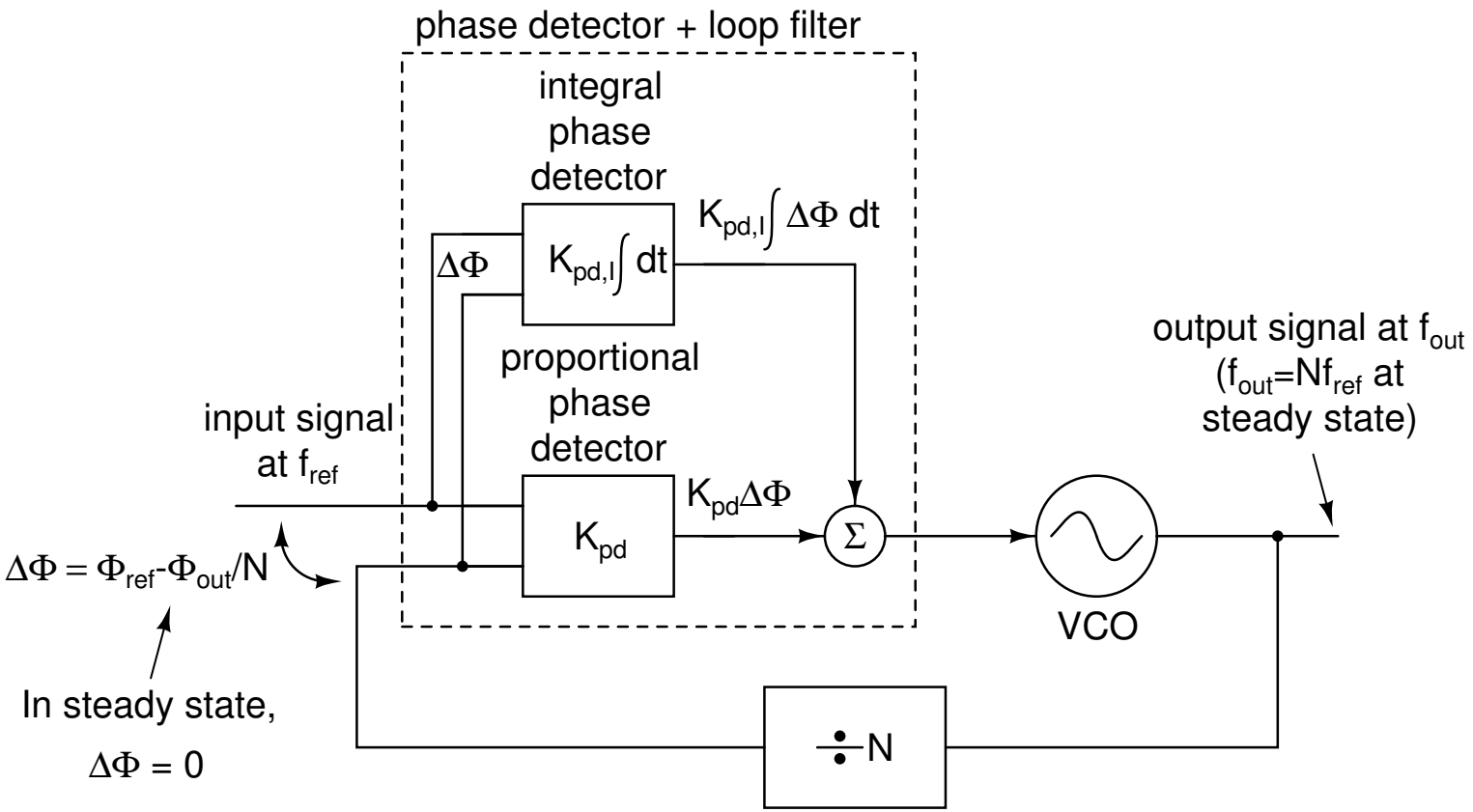
- Slowly change the bias V_{off} until $\Delta\phi = 0$

Slowly change the bias until $\Delta\phi = 0$



- Measure $\Delta\phi$ and integrate it to control V_{off}

Type II Phase locked loop

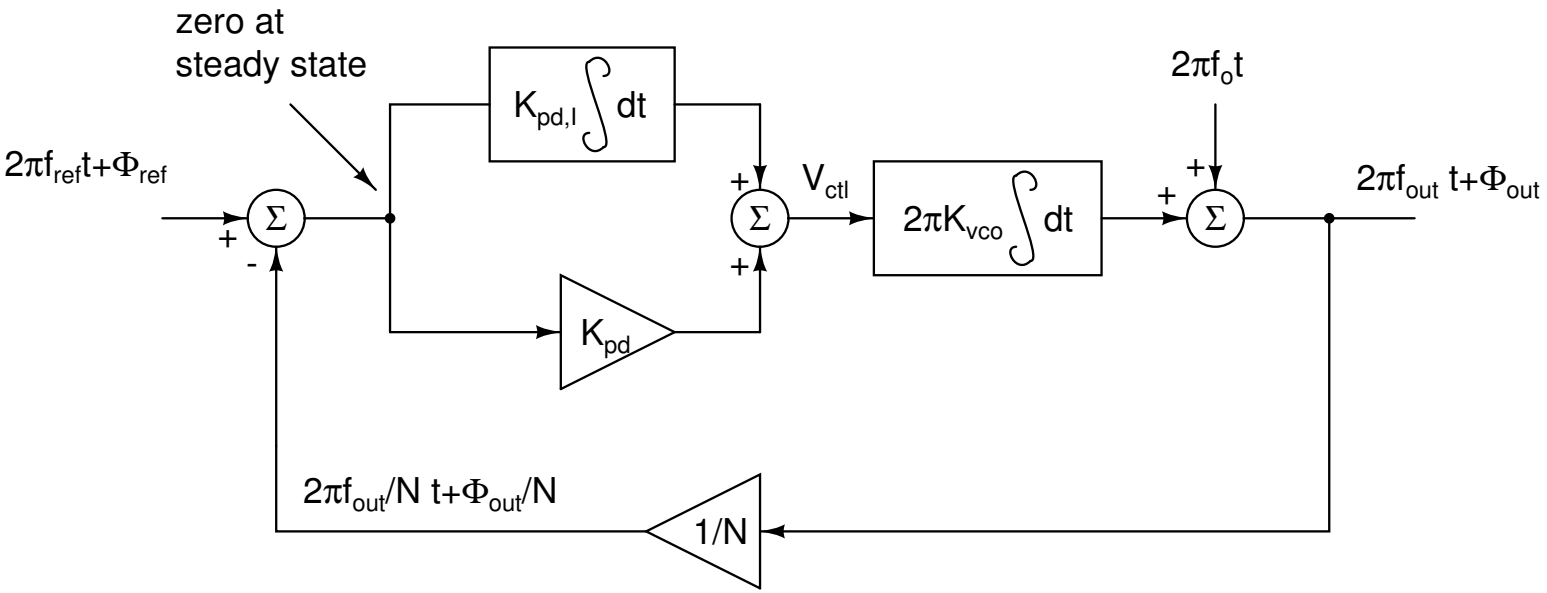


- Proportional + integral loop filter

Type II PLL with a tri state phase detector

- Lock range is not limited by the phase detector
- Loop locks with zero phase difference between reference and feedback signals
- Tri state phase detector output is zero for zero input phase difference $\Rightarrow$ No reference feedthrough!
- Reference feedthrough does exist in reality due to mismatches

Type II PLL—phase model

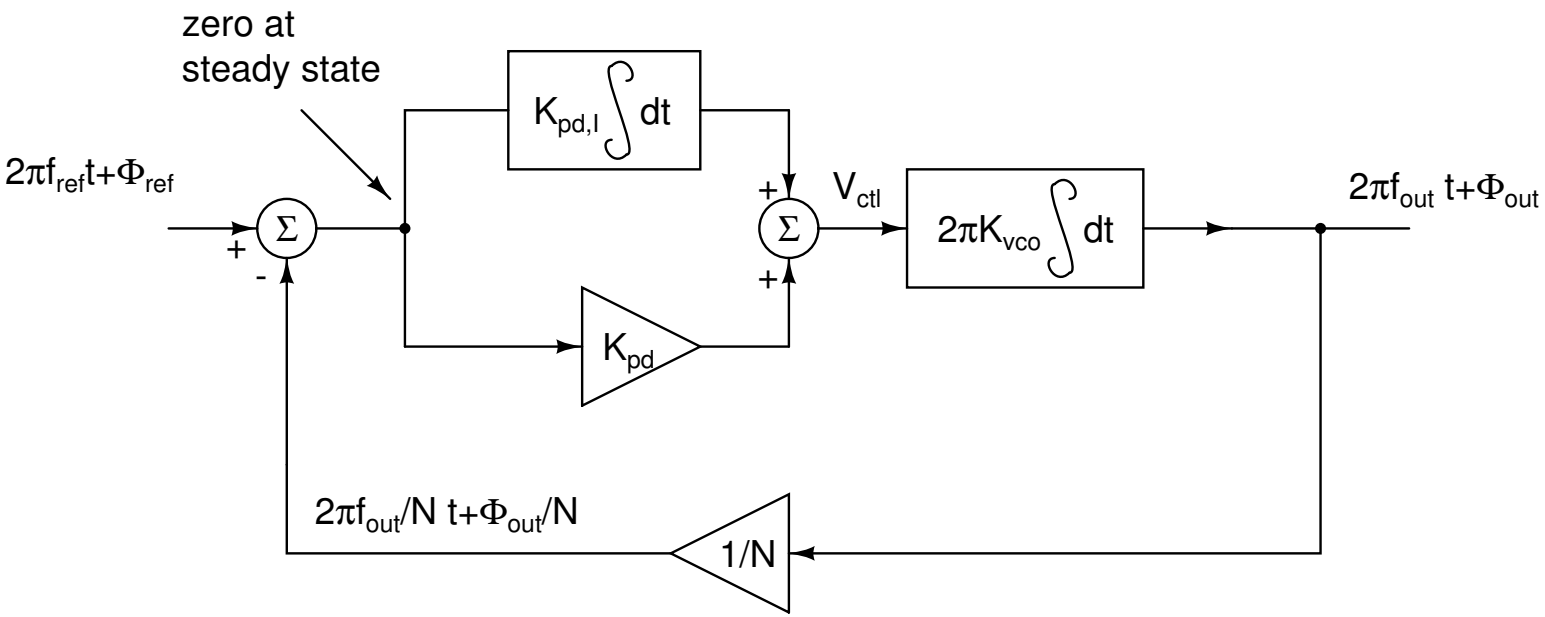


$dV_{ctl}/dt\ \alpha\ 2\pi(f_{ref}-f_{out}/N)t + \Phi_{ref} - \Phi_{out}/N$

At steady state, $f_{ref}=f_{out}/N$; $\Phi_{ref} - \Phi_{out}/N = 0$;

- Proportional + integral loop filter

Type II PLL—incremental model

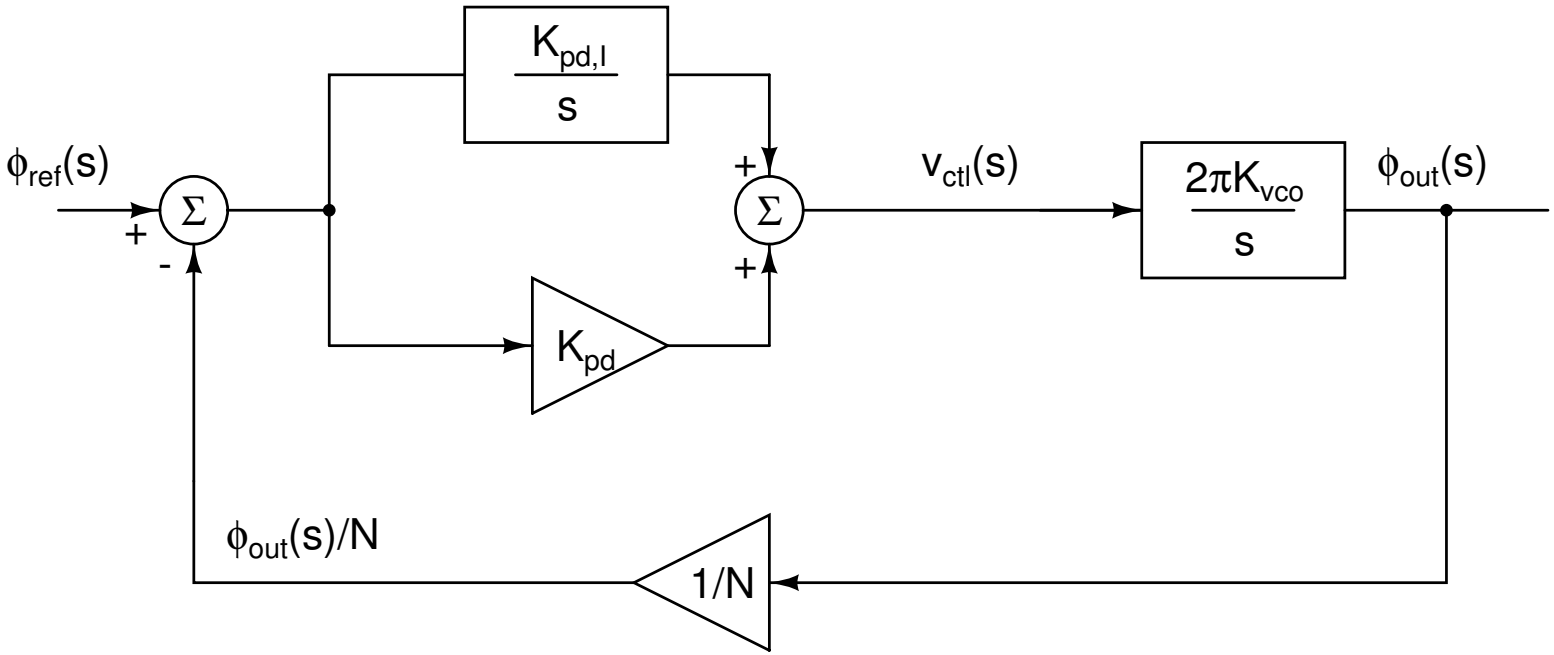


$dV_{ctl}/dt\ \alpha\ 2\pi(f_{ref}-f_{out}/N)t + \Phi_{ref} - \Phi_{out}/N$

At steady state, $f_{ref}=f_{out}/N$; $\Phi_{ref} - \Phi_{out}/N = 0$;

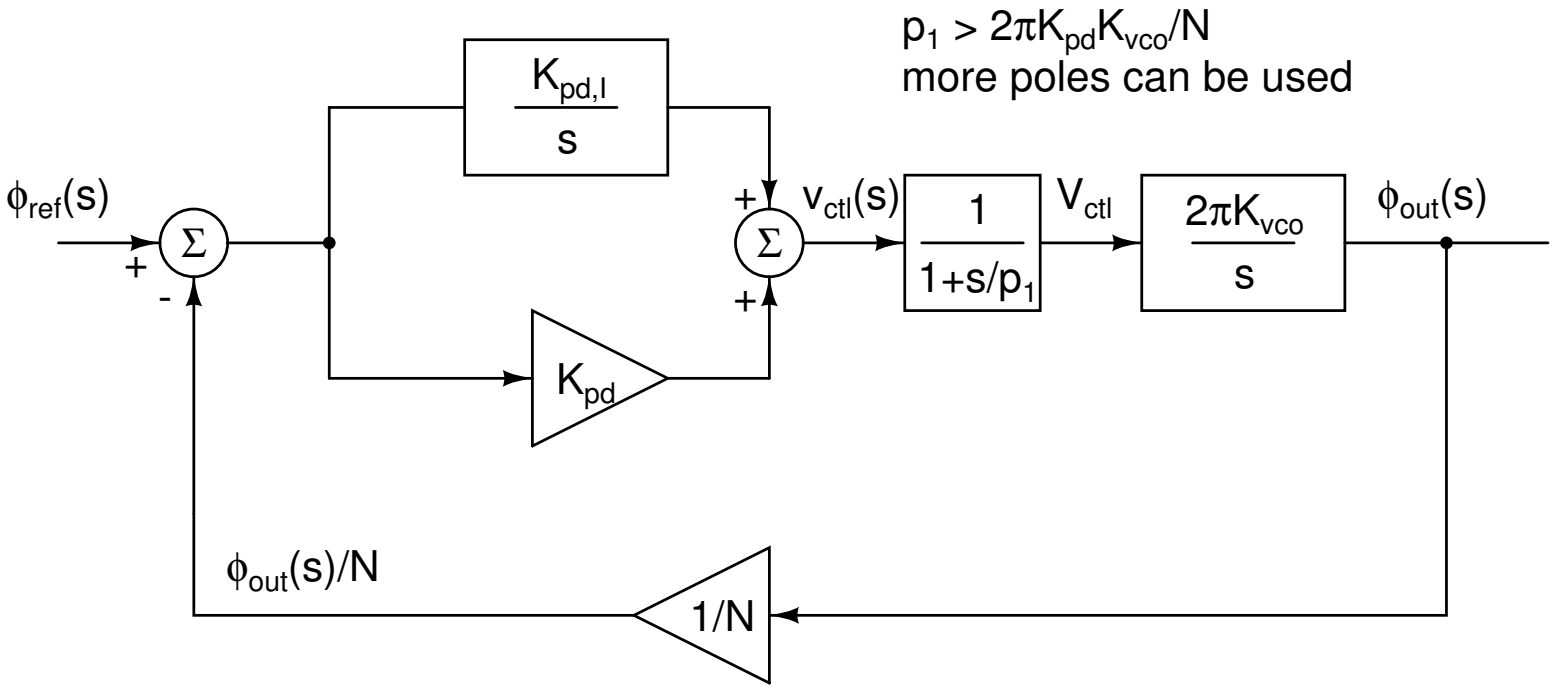
- Proportional + integral loop filter

Type II PLL—incremental model

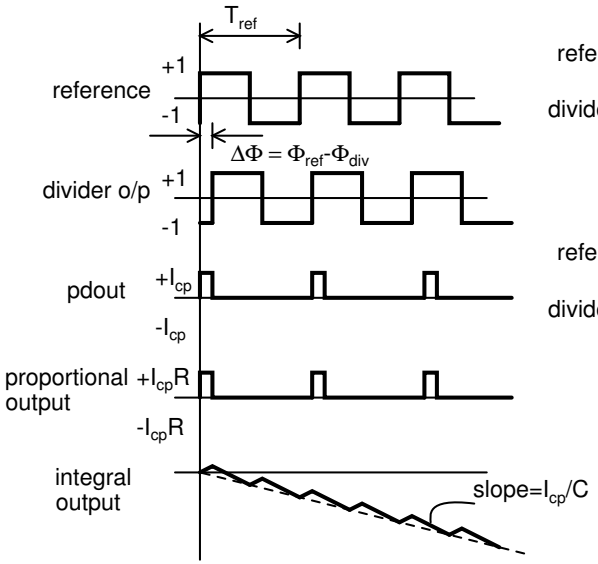


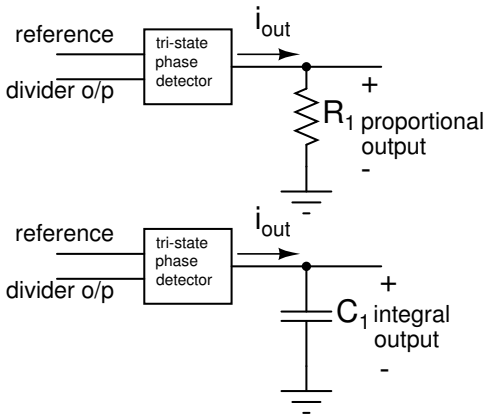
- Proportional + integral loop filter

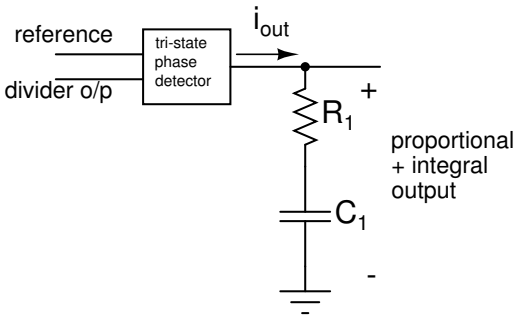
Type II PLL—Frequency domain



Type II PLL—Implementation

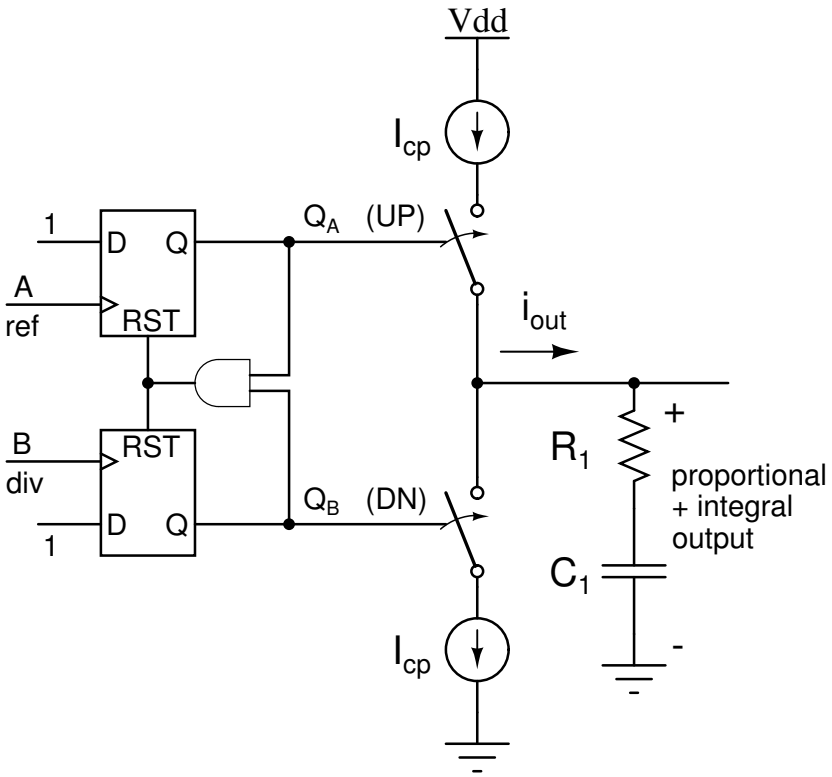






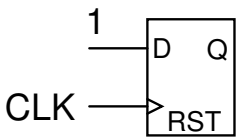
- Phase detector with a current output ($\pm I_{cp}$)
- Integral term $K_{pd,I}/s$: Current flowing into a capacitor C_1
- Proportional term K_{pd}: Current flowing into a resistor R_1
- Series RC to obtain the sum
- $K_{pd} = I_{cp}R_1/2\pi$; $K_{pd,I} = I_{cp}C_1/2\pi$

Tri state phase detector with charge pump

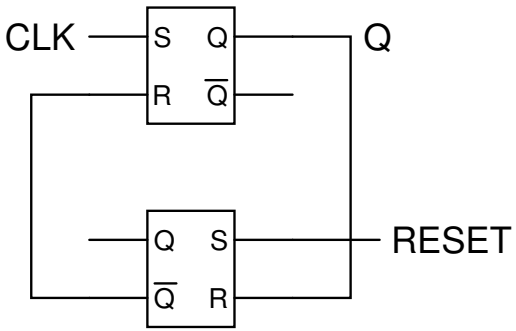


- Q_A and Q_B drive a charge pump
- Charge driven into the loop filter $I_{cp} T_{ref} \Delta\Phi / 2\pi$

Tri state phase detector implementation example

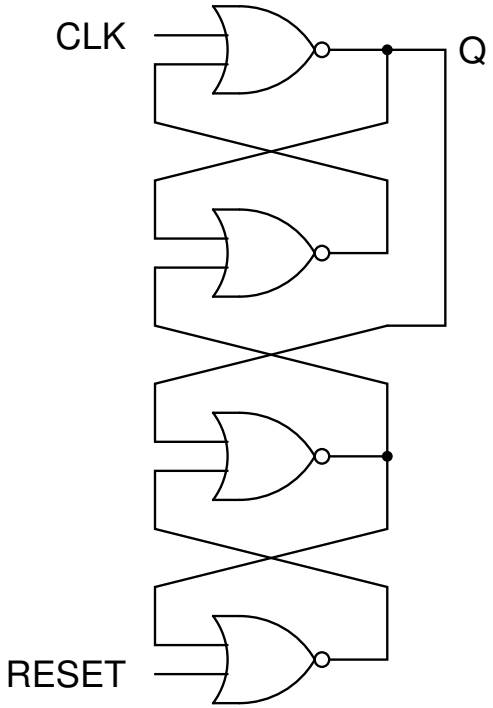


D latch with reset and D="1"



(D input with "1" implicit)

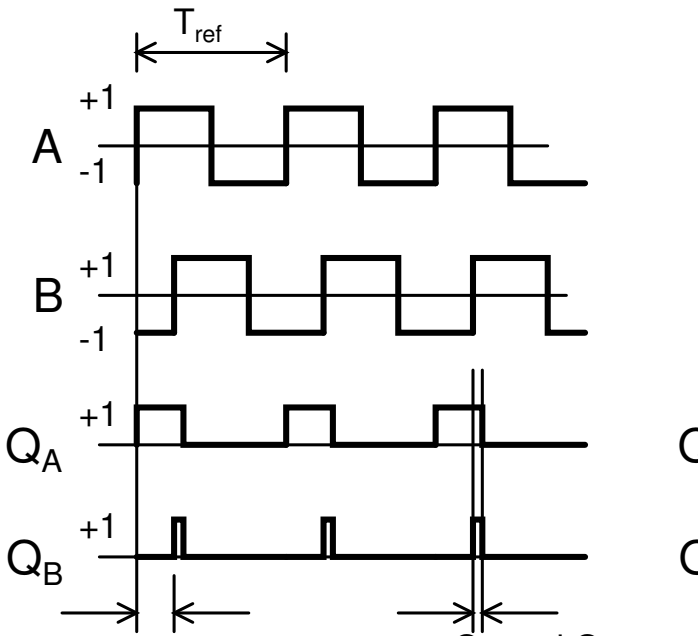
Realization using SR latches

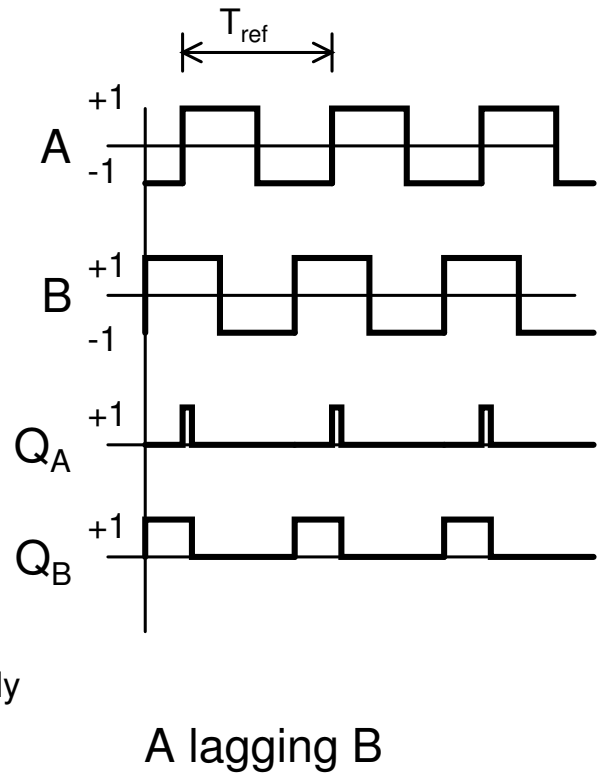


Realization using NOR gates

- D flip flops with reset implemented using SR latches

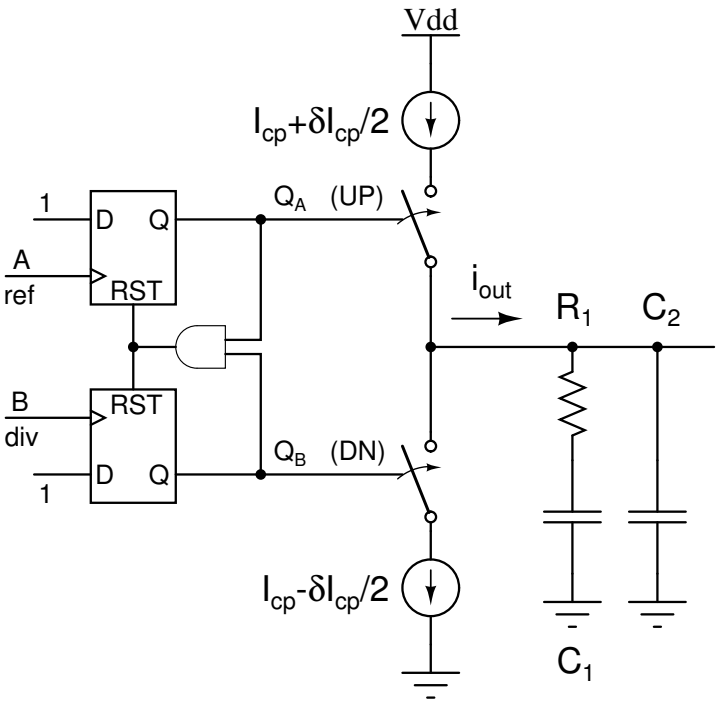
Tri state phase detector-reset path delay

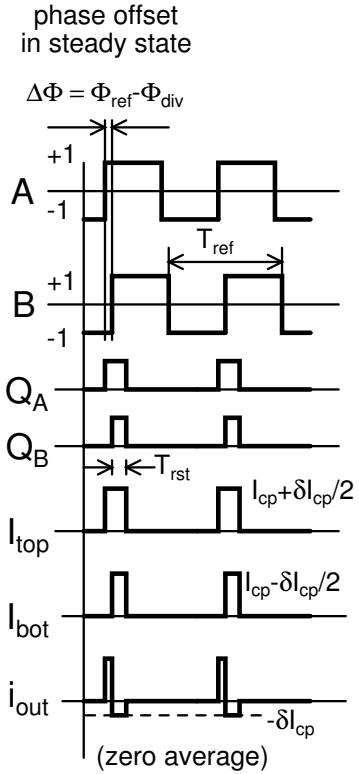




- Q_A and Q_B simultaneously high for a short duration
- $Q_A - Q_B$ proportional to $\Delta\Phi$

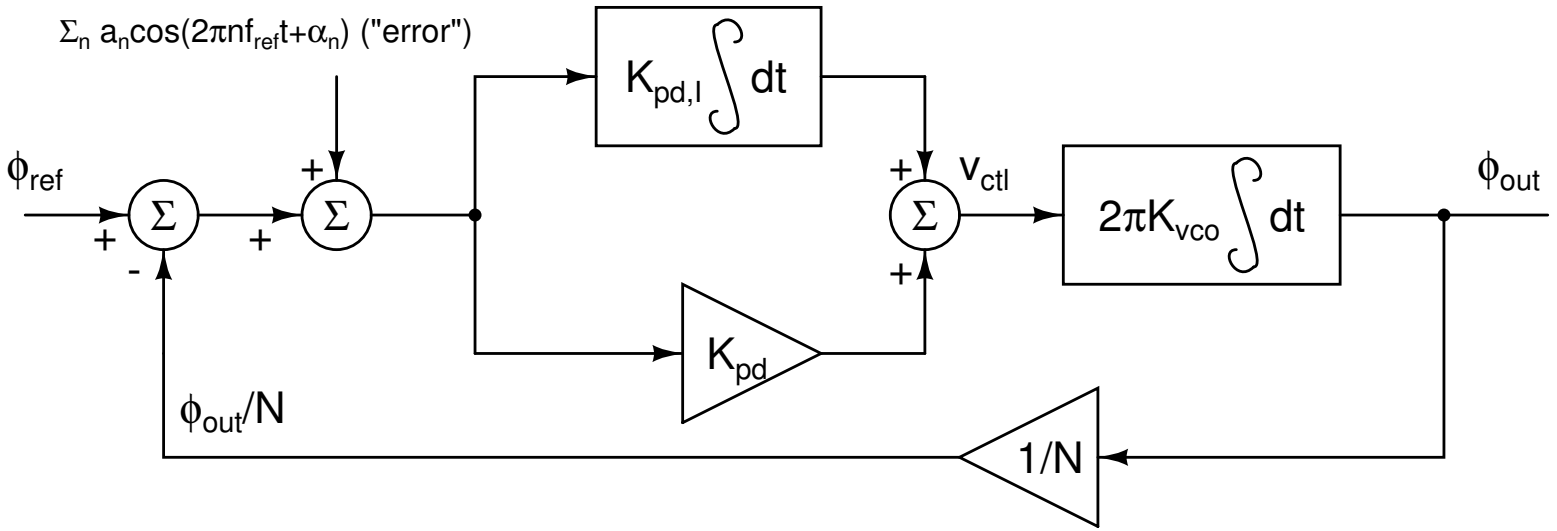
Tri state phase detector-current source mismatch





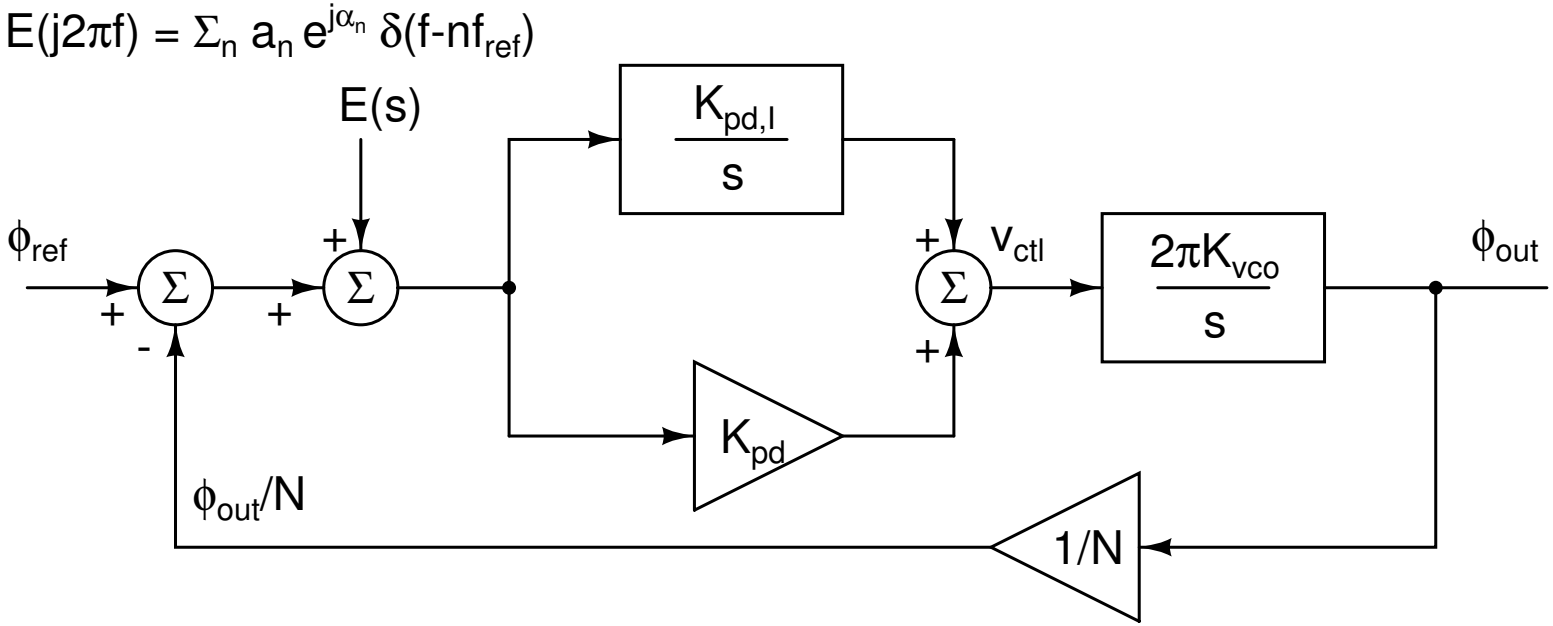
- Ideally $\Delta\Phi = 0$ in a type-II loop $\Rightarrow$ no ref. feedthrough
- Mismatch between top and bottom current sources and switching transients causes a non zero $\Delta\Phi$ and reference feedthrough
- Current pulse area $\propto \delta I_{cp} T_{rst}$ much smaller than in a Type I PLL (area $\sim I_{cp} T_{ref}$)

Type II PLL with a tri state phase detector

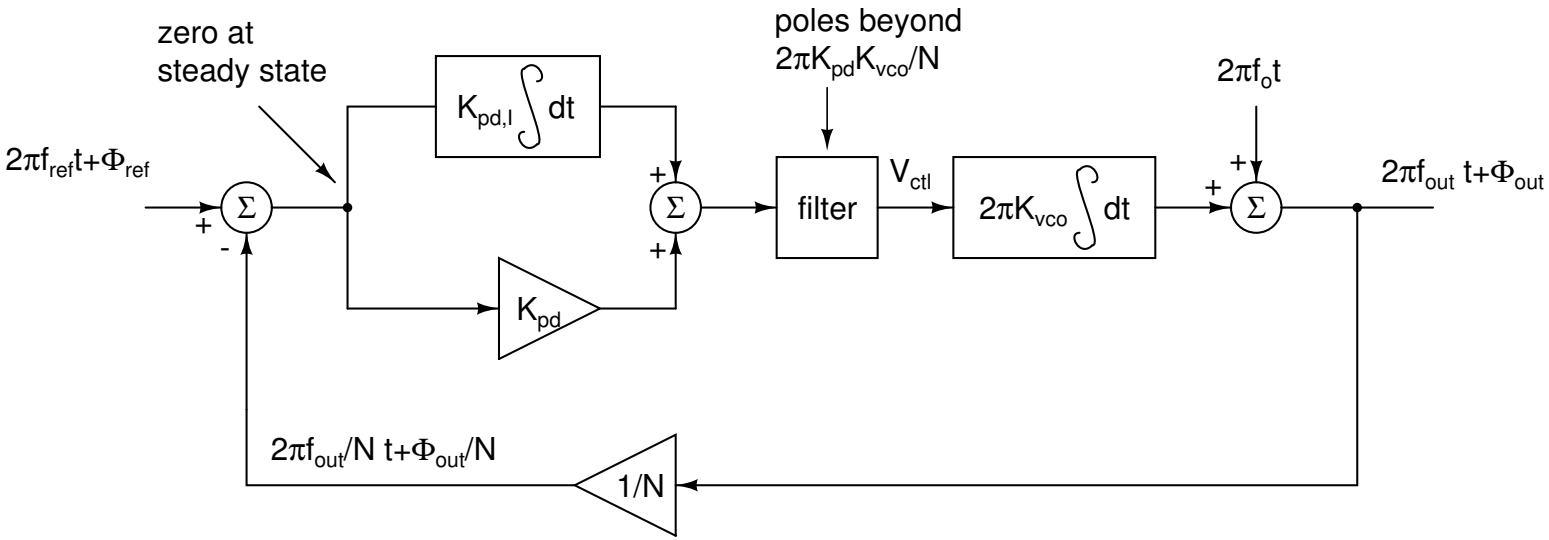


- Loop locks with a small phase offset (due to mismatch) between ϕ_{ref} and ϕ_{vco}/N for all frequencies
- Error $E(t)$ is periodic at f_{ref}: $E(t) = \sum_{n=1}^{\infty} a_n \cos(2\pi n f_{ref} t + \alpha_n)$
- Amplitude of $E(t)$ related to mismatch; much smaller than in a type-I PLL

Type II PLL with a tri state phase detector-Frequency domain



Type II PLL—Additional attenation poles

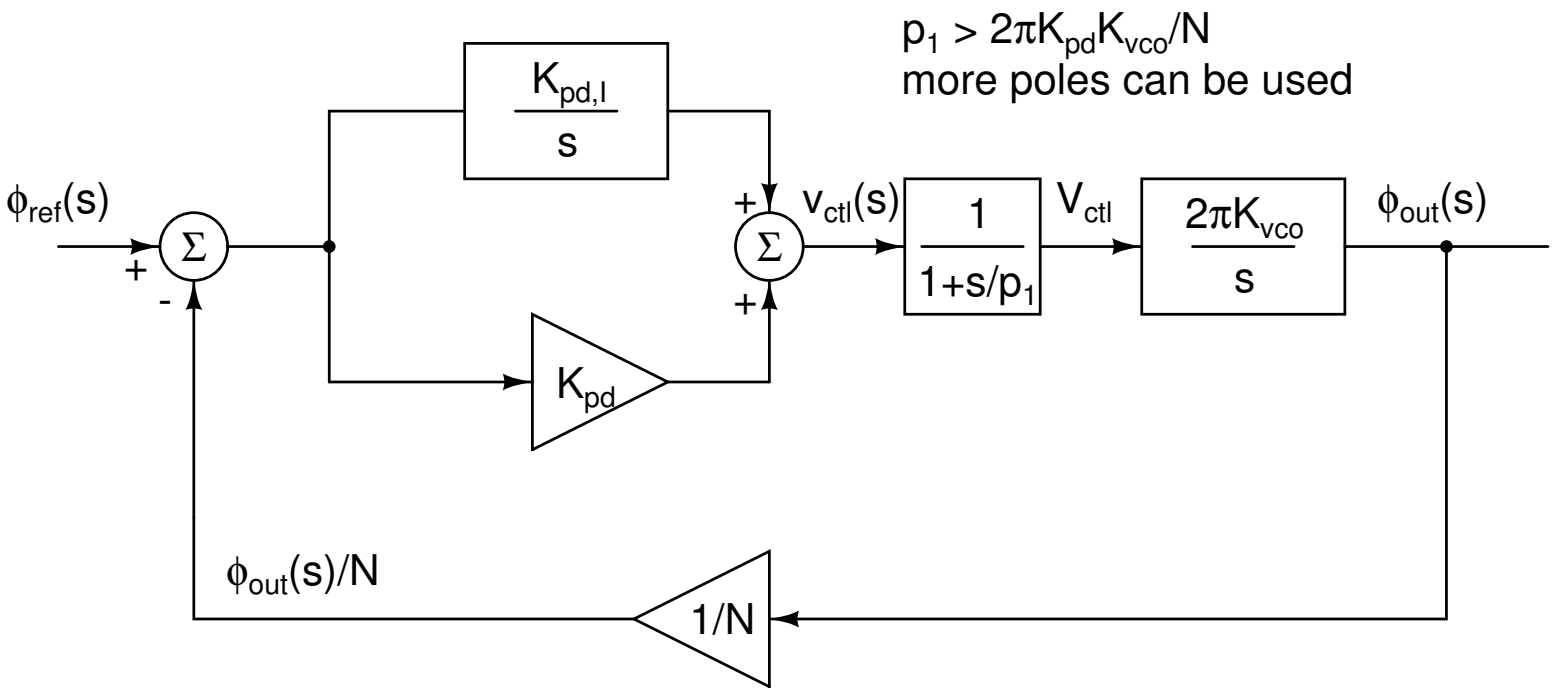


$dV_{ctl}/dt \; \alpha \; 2\pi(f_{ref}-f_{out}/N)t + \Phi_{ref} - \Phi_{out}/N$

At steady state, $f_{ref}=f_{out}/N$; $\Phi_{ref} - \Phi_{out}/N = 0$;

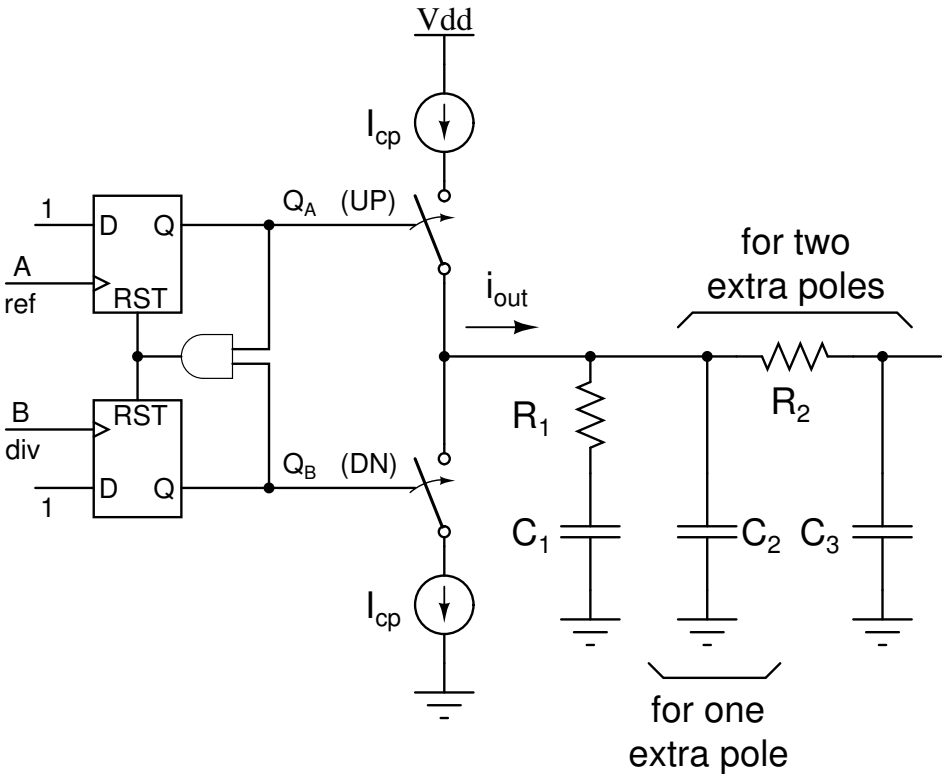
- Additional poles beyond the unity loop gain frequency to reduce reference feedthrough

Type II PLL—Additional attenation poles



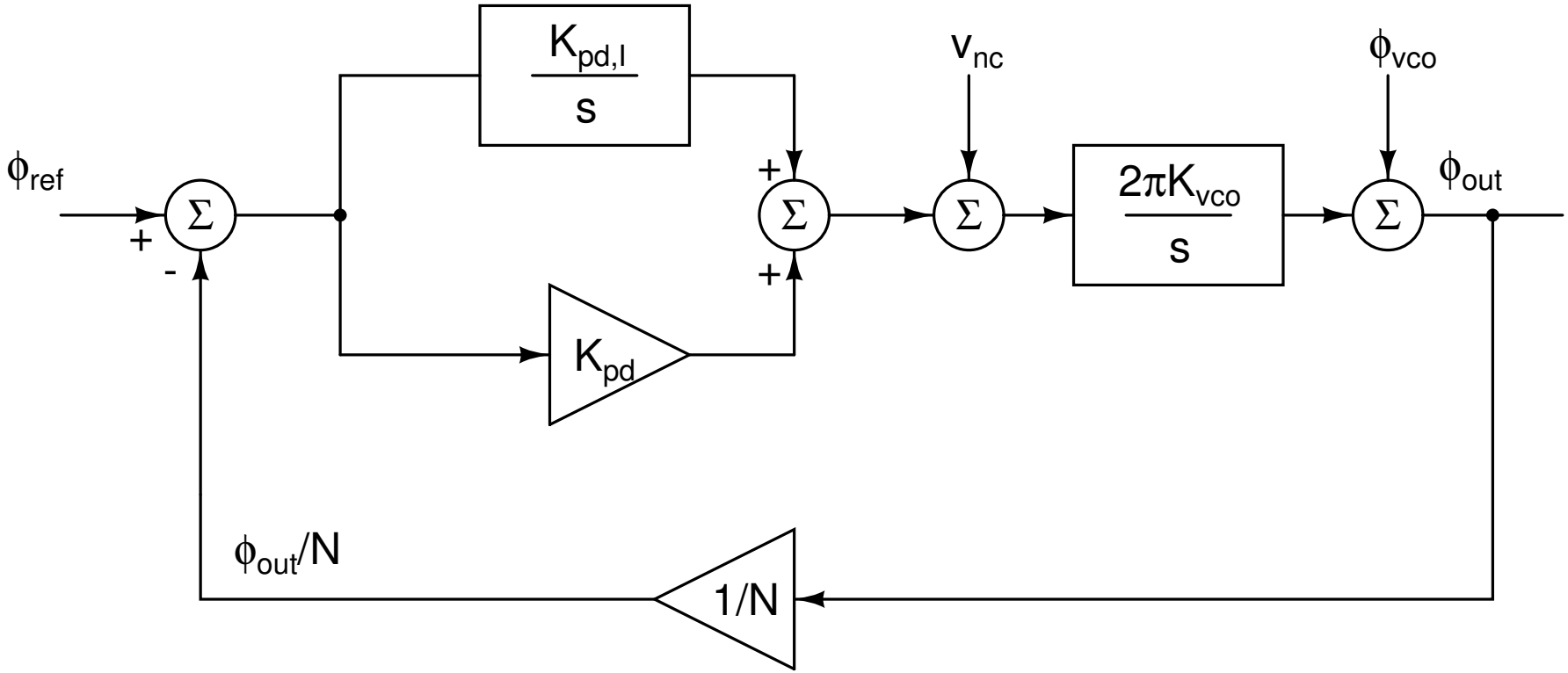
- Additional poles beyond the unity loop gain frequency to reduce reference feedthrough

Type II PLL—Additional attenation poles



- Extra RC sections for additional poles
- Must be sufficiently beyond the unity loop gain frequency to ensure sufficient phase margin

Noise sources in a PLL



- Noise can be added as ϕ_{ref} (reference phase noise, charge-pump noise, divider output phase noise) or v_{nc} (loop filter noise) or ϕ_{vco} (VCO phase noise)
- Need to compute transfer functions from each of these noise sources to ϕ_{out}

Type-II PLL: transfer functions

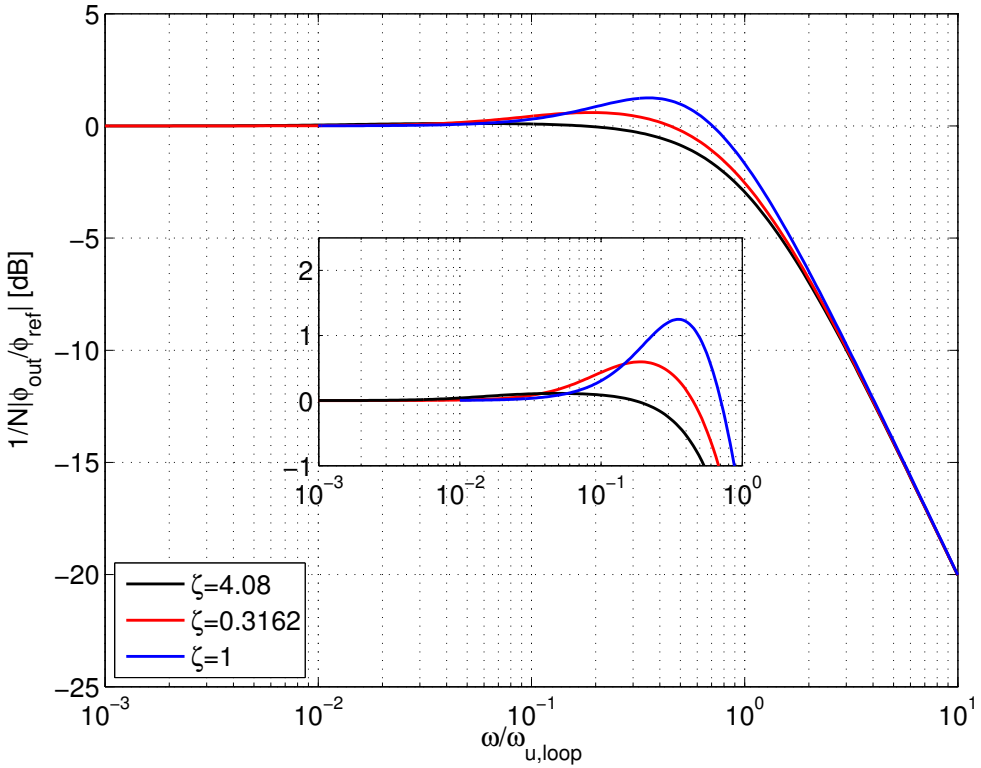
$$
\begin{aligned}
L(s) &= \frac{\omega_{u,loop}}{s}\frac{z_1}{s}\left(1+\frac{s}{z_1}\right) \\
\omega_{u,loop} &= \frac{2\pi K_{pd}K_{vco}}{N} = \frac{I_{cp}RK_{vco}}{N} \\
z_1 &= \frac{K_{pd,I}}{K_{pd}} = \frac{1}{RC} \\
\frac{\phi_{out}(s)}{\phi_{ref}(s)} &= N\frac{1+s/z_1}{1+s/z_1+s^2/z_1\omega_{u,loop}} \\
\frac{\phi_{out}(s)}{V_{nc}(s)} &= \frac{N}{K_{pd}}\frac{s/z_1}{1+s/z_1+s^2/z_1\omega_{u,loop}} \\
\frac{\phi_{out}(s)}{\phi_{vco}(s)} &= \frac{s^2/z_1\omega_{u,loop}}{1+s/z_1+s^2/z_1\omega_{u,loop}}
\end{aligned}
$$

Type-II PLL: transfer functions

$$\frac{L(s)}{1+L(s)} = \frac{1+s/z_1}{1+s/z_1+s^2/z_1\omega_{u,loop}}$$

- Two poles and a zero
- Zero $z_1 = K_{pd,I}/K_{pd}$
- Natural frequency $\omega_n = \sqrt{2\pi K_{pd,I}K_{vco}/N}$
- Quality factor $Q = \sqrt{z_1/\omega_{u,loop}} = \sqrt{NK_{pd,I}/2\pi K_{vco}}/K_{pd}$
- Damping factor $\zeta = 1/2Q = 1/2\sqrt{\omega_{u,loop}/z_1}$
- For well separated (real) poles ($z_1 \ll \omega_{u,loop}$), $p_1 \approx z_1 + z_1^2/\omega_{u,loop} \approx z_1$, $p_2 \approx \omega_{u,loop} - z_1$,
- Pole zero doublet $\{p_1, z_1\}$; p_1 at a slightly higher frequency than z_1

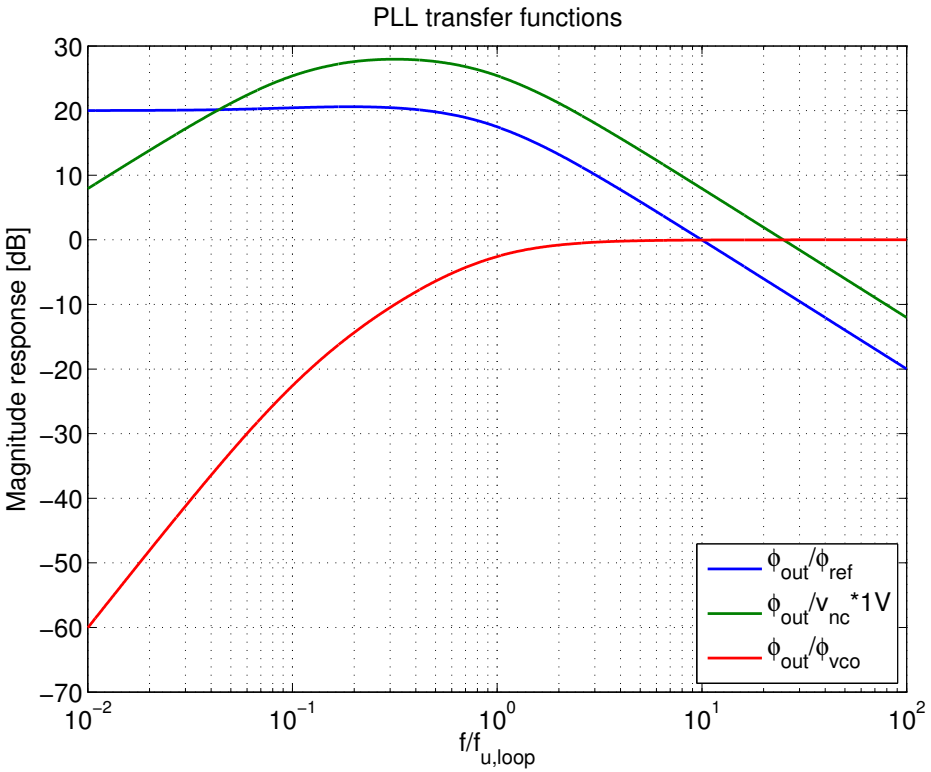
Type-II PLL: transfer functions



$$\frac{\phi_{out}(s)}{\phi_{ref}(s)} = N\frac{1+s/z_1}{1+s/z_1+s^2/z_1\omega_{u,loop}}$$

- Peaking in $|\phi_{out}/\phi_{ref}|$ because of the zero
- Damping factor $\zeta \gg 1$ to avoid peaking $\Rightarrow$ slow settling

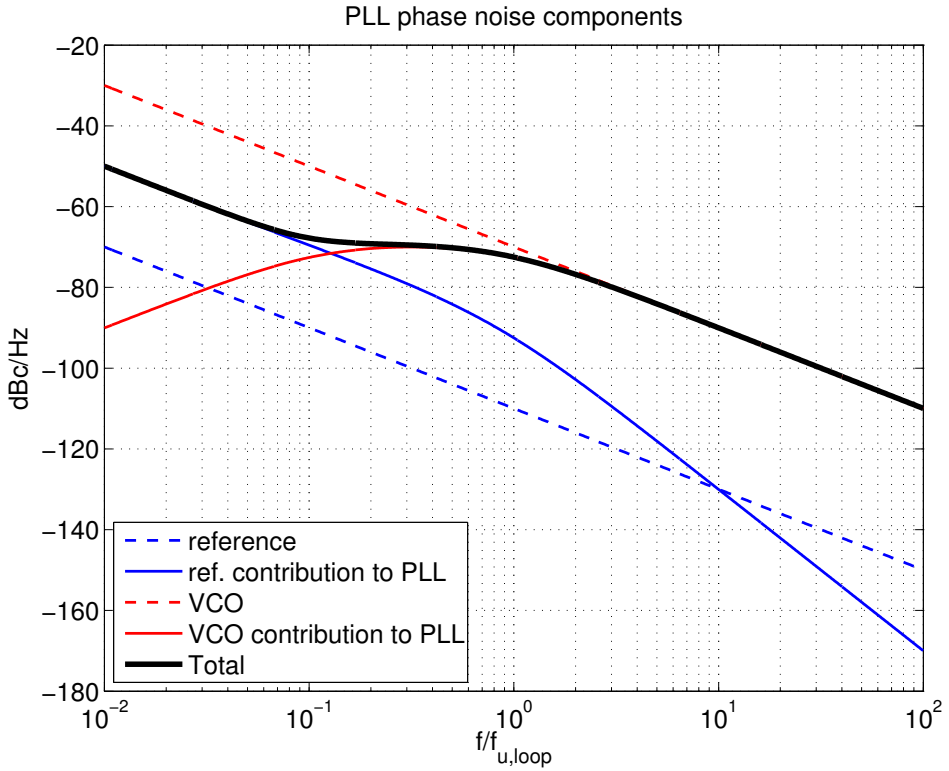
Type-II PLL: transfer functions



(Example parameters:
$N = 10, z_1 = 0.1\omega_{u,loop}, N/K_{pd} = 2\pi K_{vco}/\omega_{u,loop} = 25\,\mathrm{V}^{-1}$)

- $|\phi_{out}/\phi_{ref}|$: Lowpass with a dc gain N
- $|\phi_{out}/v_{nc}|$: Bandpass with peak gain $N/K_{pd} = 25\,\mathrm{V}^{-1}$
- $|\phi_{out}/\phi_{vco}|$: Highpass with a high frequency gain of 1

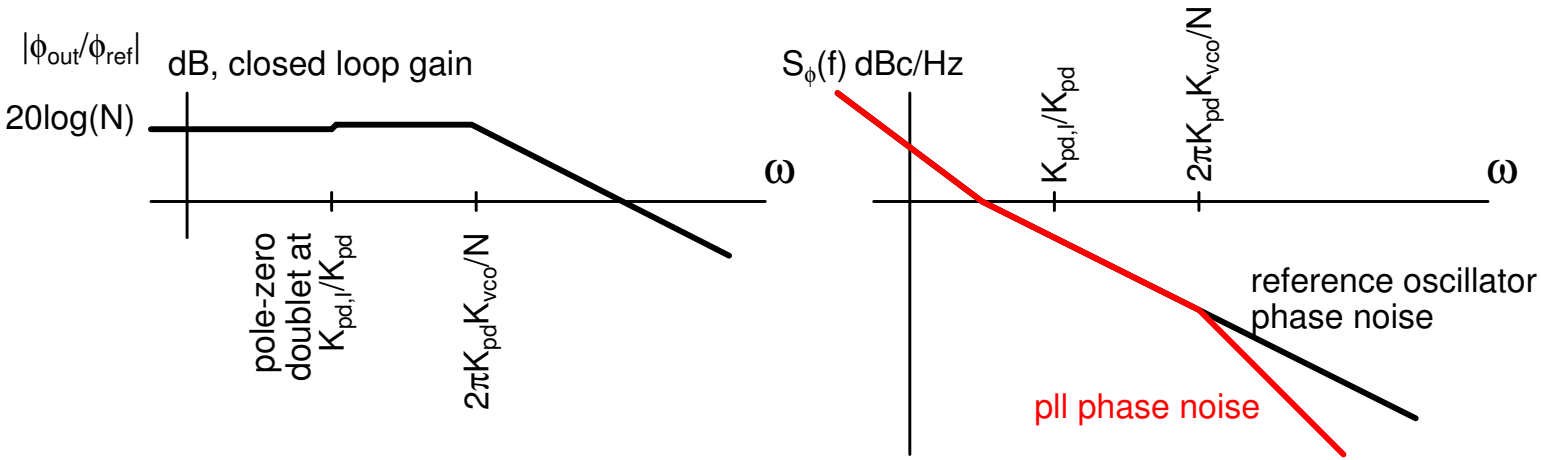
Type-II PLL phase noise example



(Example parameters:
$N = 10, z_1 = 0.1\omega_{u,loop}, N/K_{pd} = 2\pi K_{vco}/\omega_{u,loop} = 25\,\mathrm{V}^{-1}$)

- Reference contribution dominant below $0.1\omega_{u,loop}$
- VCO contribution dominant above $0.1\omega_{u,loop}$
- VCO contribution reduced by the loop upto $\omega_{u,loop}$
- Charge pump and loop filter noise ignored in the above

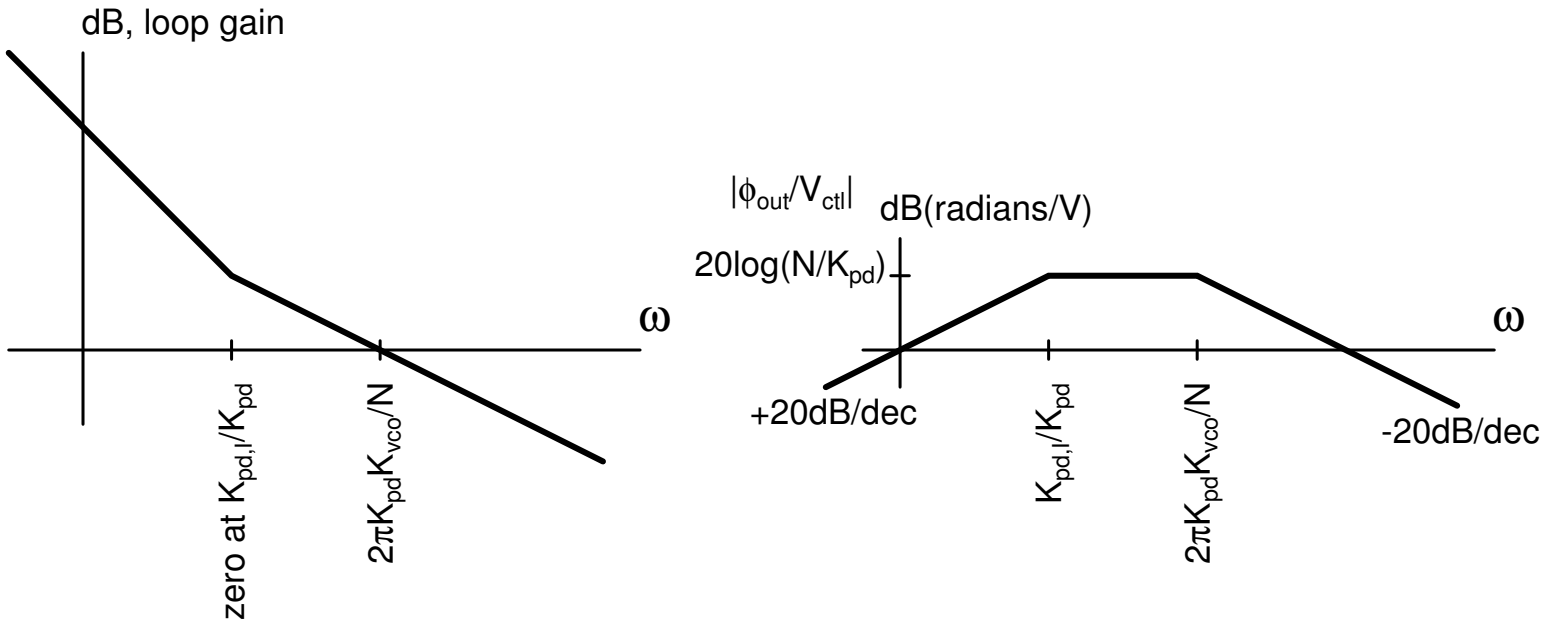
Type-II PLL: Reference input



$$\frac{\phi_{out}(s)}{\phi_{ref}(s)} = N\frac{1+sK_{pd}/K_{pd,I}}{s^2\frac{N}{2\pi K_{pd,I}K_{vco}}+s\frac{K_{pd}}{K_{pd,I}}+1}$$

- Low pass response; Reference noise attenuated at high frequencies
- Low frequency gain of N, -3 dB bandwidth of $2\pi K_{pd}K_{vco}/N$
- Pole zero doublet $p_1 \approx z_1 = K_{pd,I}/K_{pd}$; p_1 at a slightly higher frequency than z_1

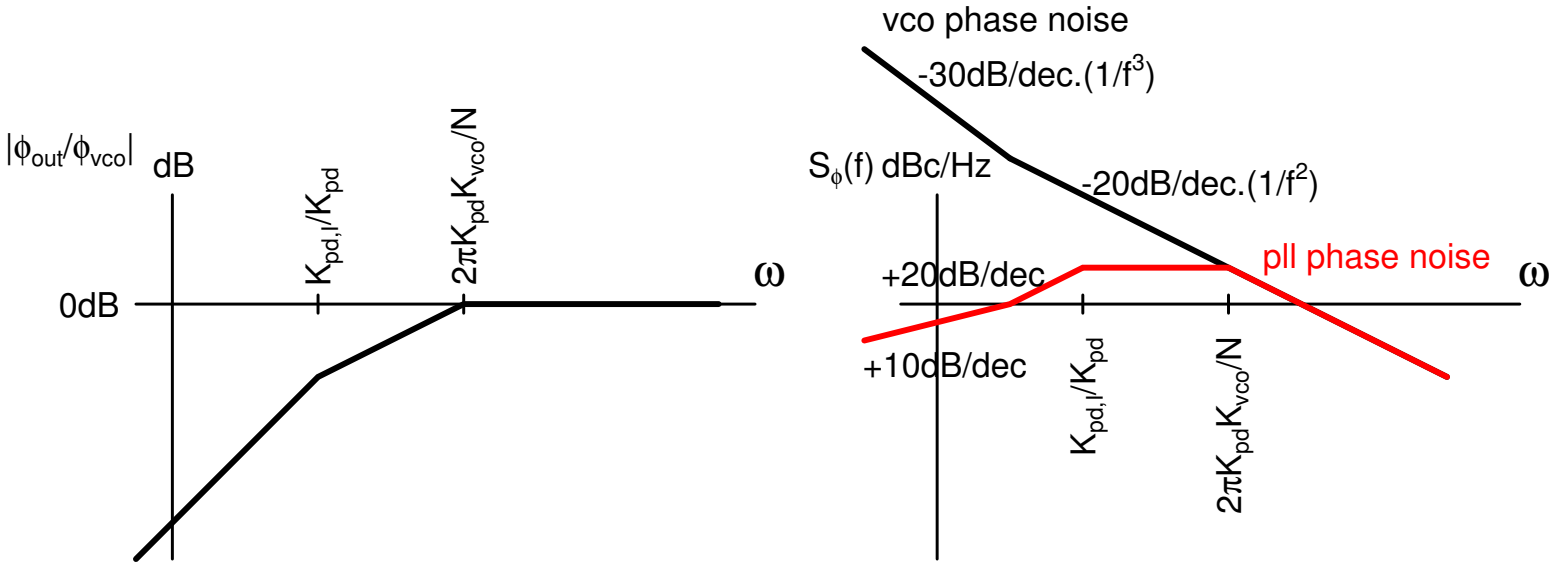
Type-II PLL: Noise added to control node



$$\frac{\phi_{out}(s)}{V_{ctl}(s)} = \frac{N}{K_{pd}} \frac{sK_{pd}/K_{pd,I}}{s^2 \frac{N}{2\pi K_{pd,I}K_{vco}} + s\frac{K_{pd}}{K_{pd,I}} + 1}$$

- radians/Volt
- Bandpass response
- Mid band gain of N/K_{pd}
- Lower cutoff at $K_{pd,I}/K_{pd}$, Upper cutoff at $2\pi K_{pd}K_{vco}/N$

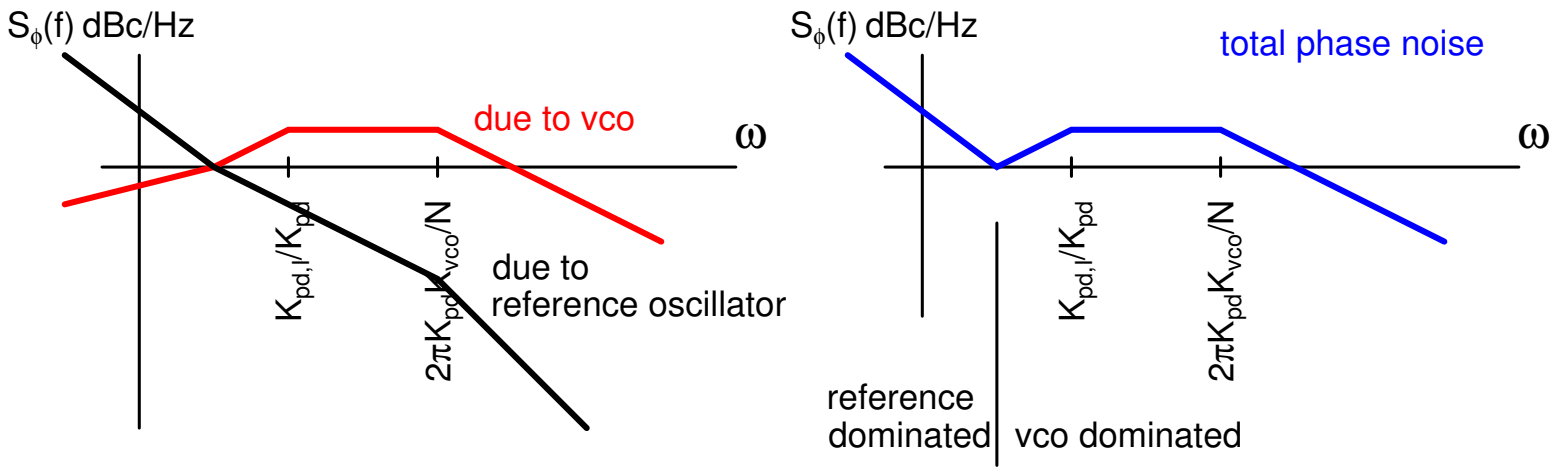
Type-II PLL: VCO noise



$$\frac{\phi_{out}(s)}{\phi_{vco}(s)} = \frac{s^2 \frac{N}{2\pi K_{pd,I} K_{vco}}}{s^2 \frac{N}{2\pi K_{pd,I} K_{vco}} + s \frac{K_{pd}}{K_{pd,I}} + 1}$$

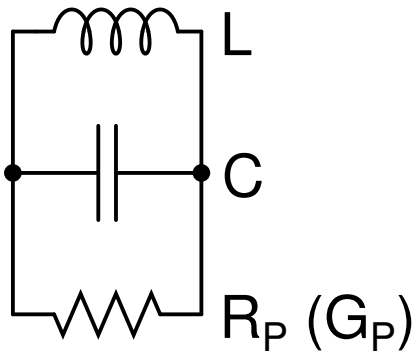
- Second order highpass response
- Feedback loop effectively inactive beyond $2\pi K_{pd} K_{vco}/N$

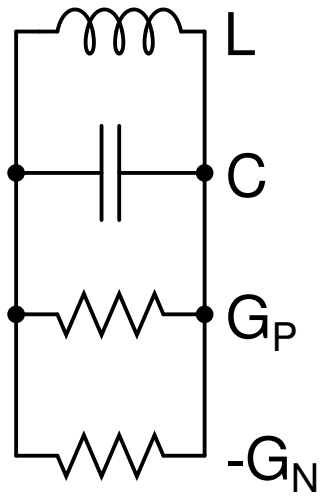
Type-II PLL phase noise example



LC oscillator

LC oscillator



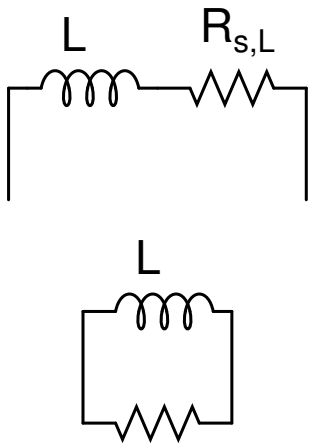


$G_N \geq G_P$

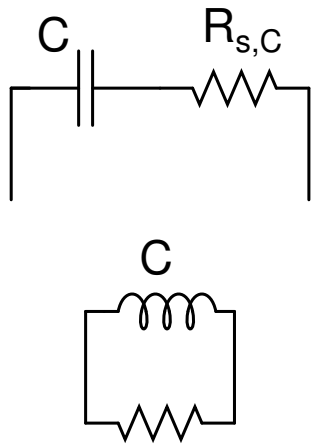
for sustained oscillation

- Lossless LC resonator sustains a sinusoidal voltage indefinitely
- LC resonator loss modeled using a parallel resistance R_p
- Compensate the loss of a lossy LC resonator using a parallel negative resistance
- Oscillation frequency $f_o = 1/2\pi\sqrt{LC}$

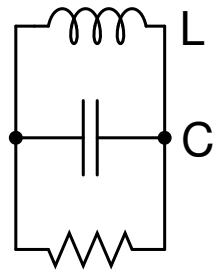
LC resonator losses



$R_{P,L} = (\omega L)^2/R_{s,L} \cong Q_L^2\, R_{s,L}$



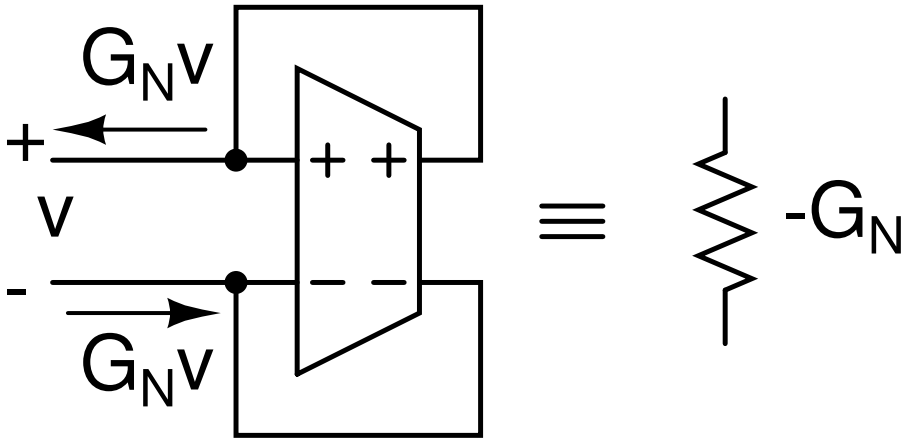
$R_{P,C} = 1/(\omega L)^2 R_{s,C} \cong Q_C^2\, R_{s,C}$



$R_P = R_{P,L} || R_{P,C}$

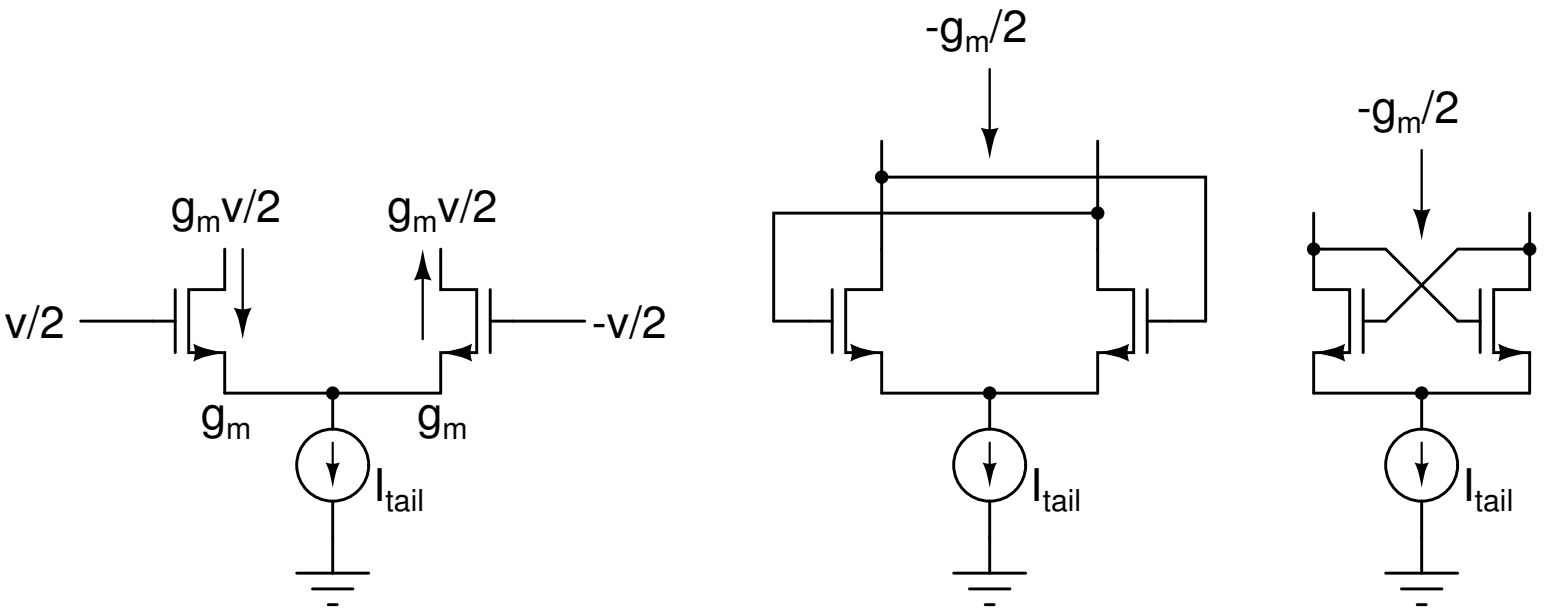
- Capacitor and Inductor series resistances represented by equivalent parallel resistances
- Effective R_p is a parallel combination of losses from all components

Negative resistance-implementation



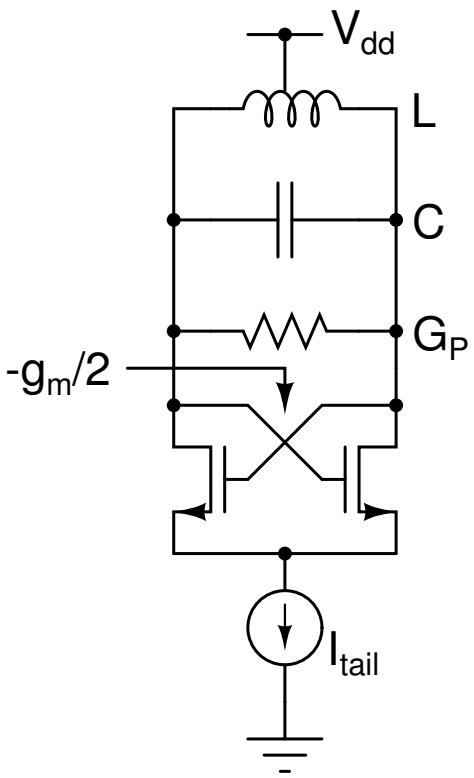
- Transconductor G_N connected in positive feedback

Negative resistance-implementation



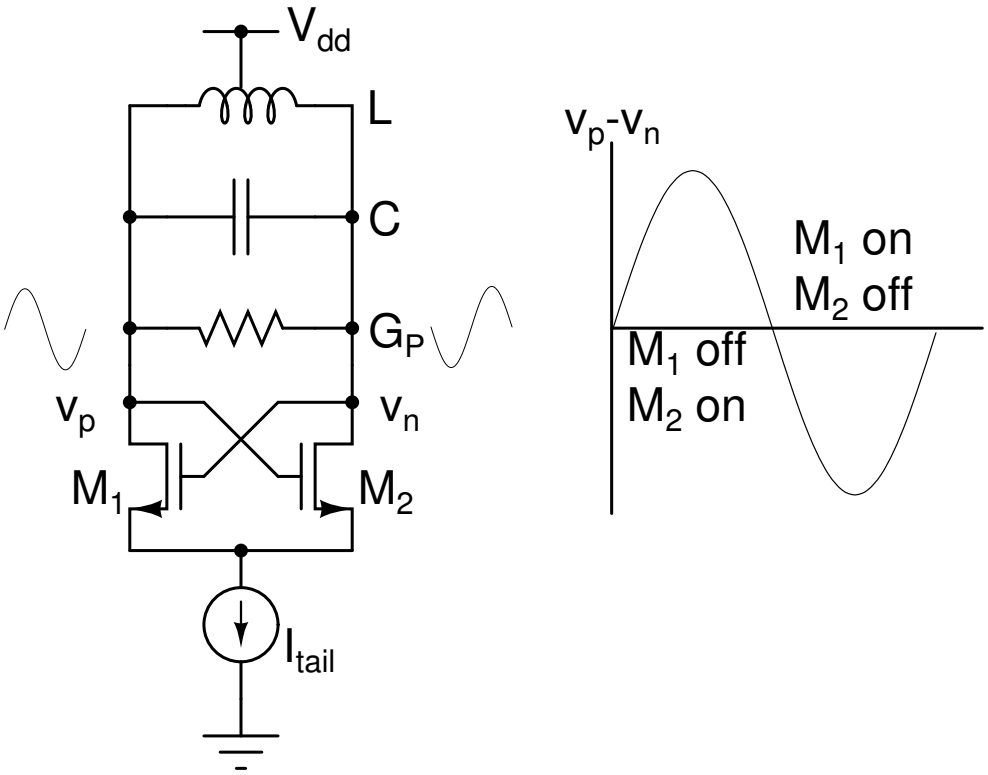
- Cross coupled differential pair
- Negative conductance $= g_m/2$ where g_m is the transconductance of each MOS device

LC oscillator



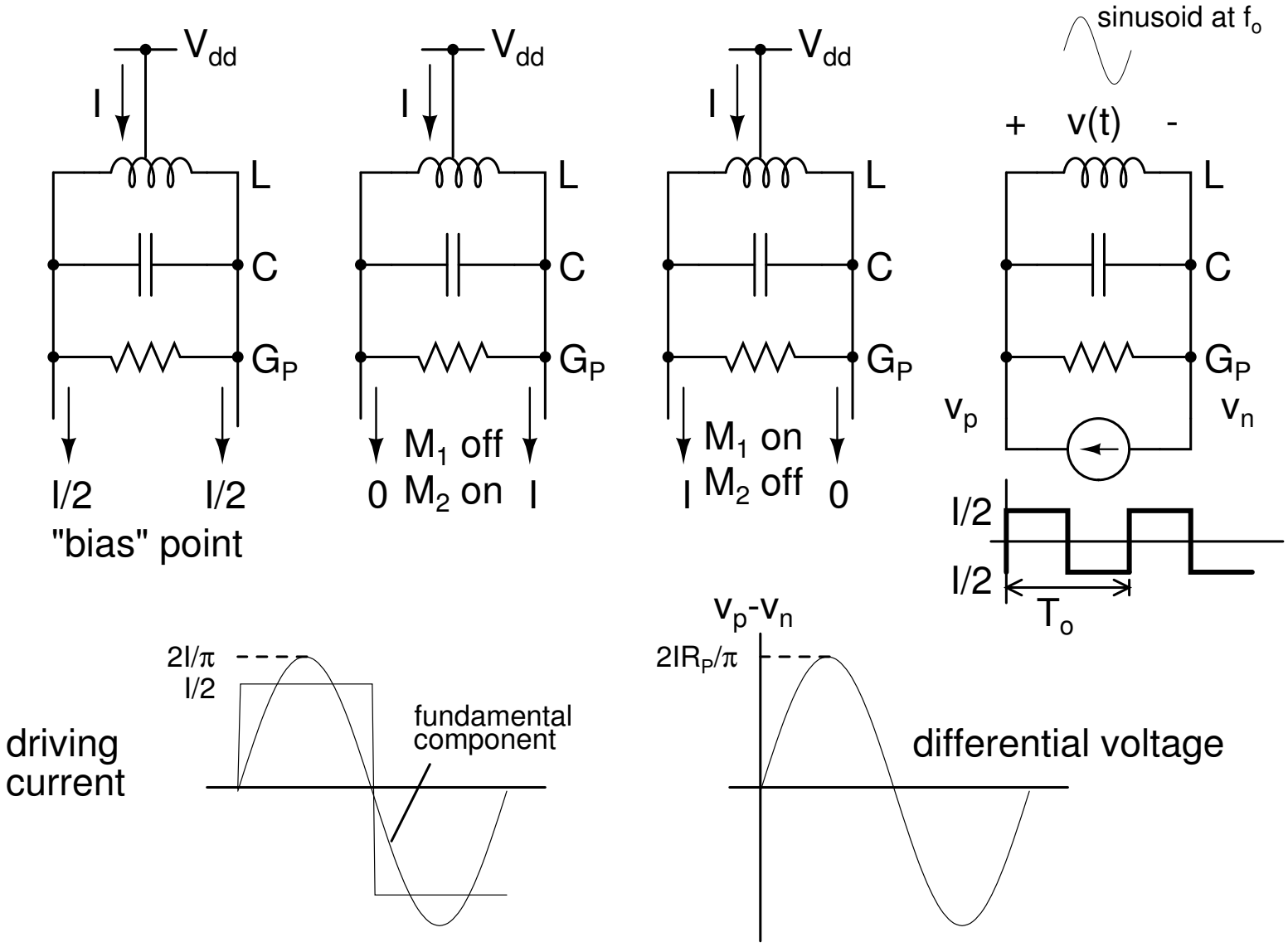
- Parallel LC tank with cross coupled differential pair
- This and its variants are the most commonly used topologies of CMOS integrated oscillators

LC oscillator-amplitude



- Complete switching of MOS devices assumed
- Equivalent to a square wave current of amplitude $I/2$ driving the parallel LC tank

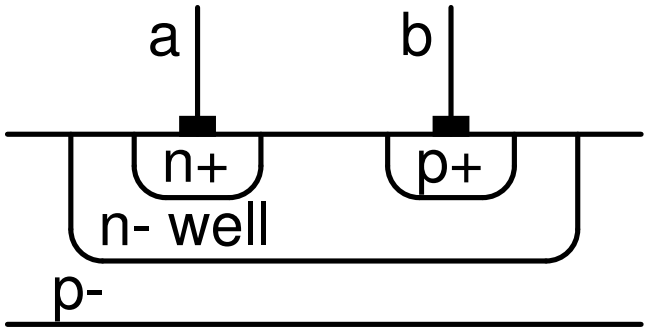
LC oscillator-amplitude

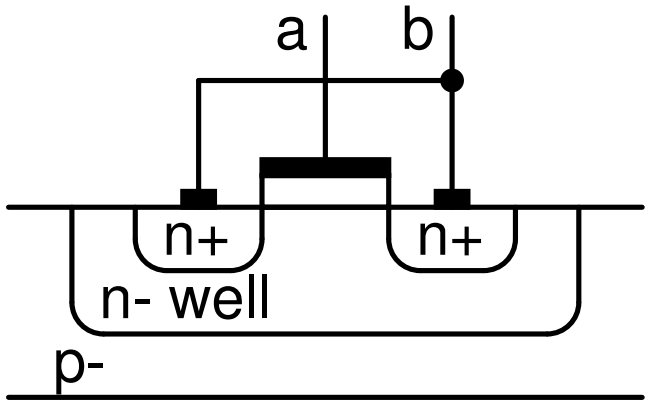


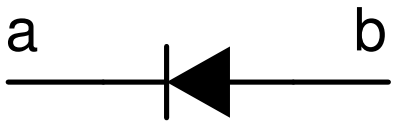
LC oscillator-amplitude

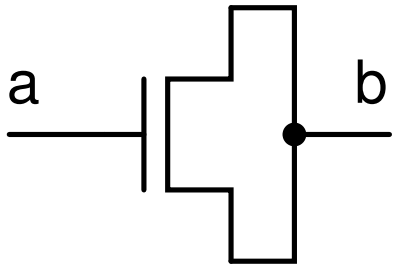
- Equivalent to a square wave current of amplitude $I/2$ driving the parallel LC tank
- All components except the fundamental filtered out
- Amplitude of the differential sinusoidal voltage = $2IR_P/\pi$

LC oscillator-tunability



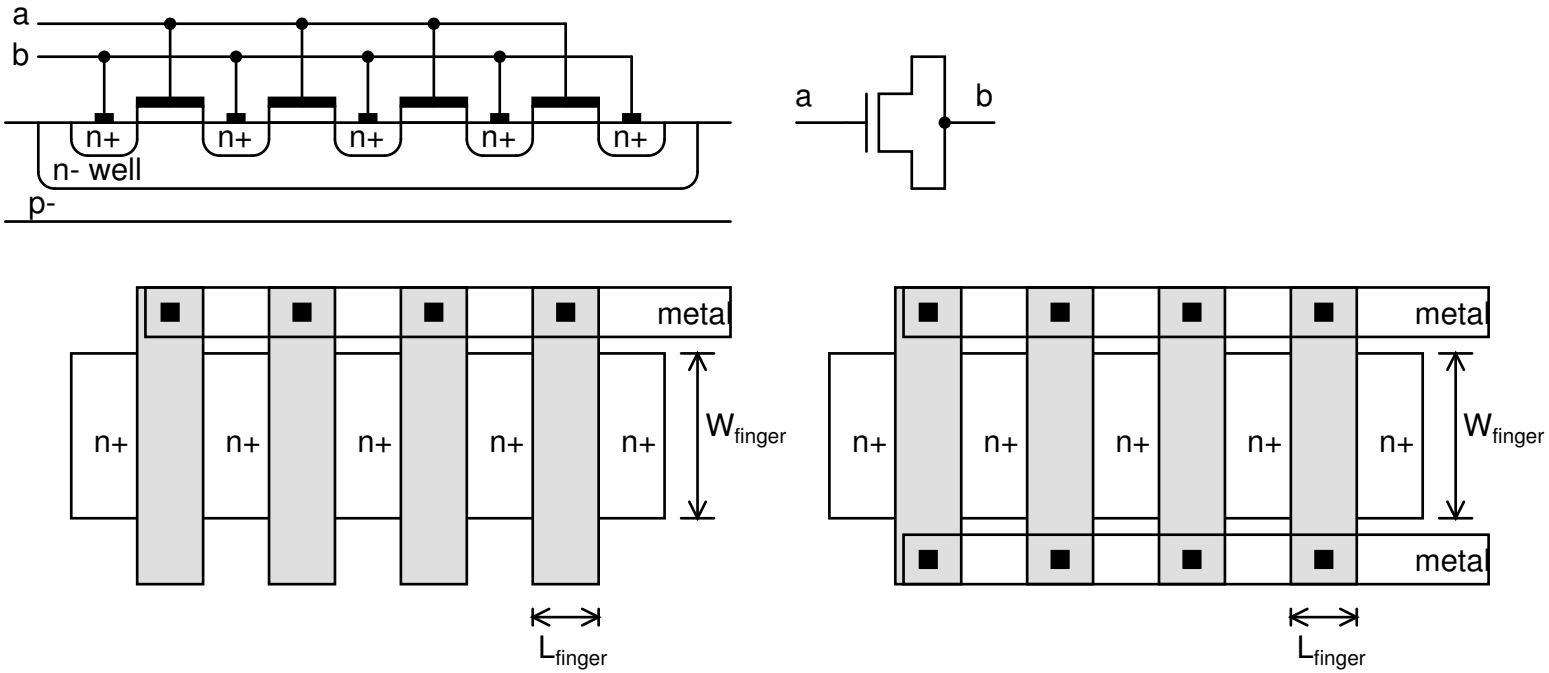






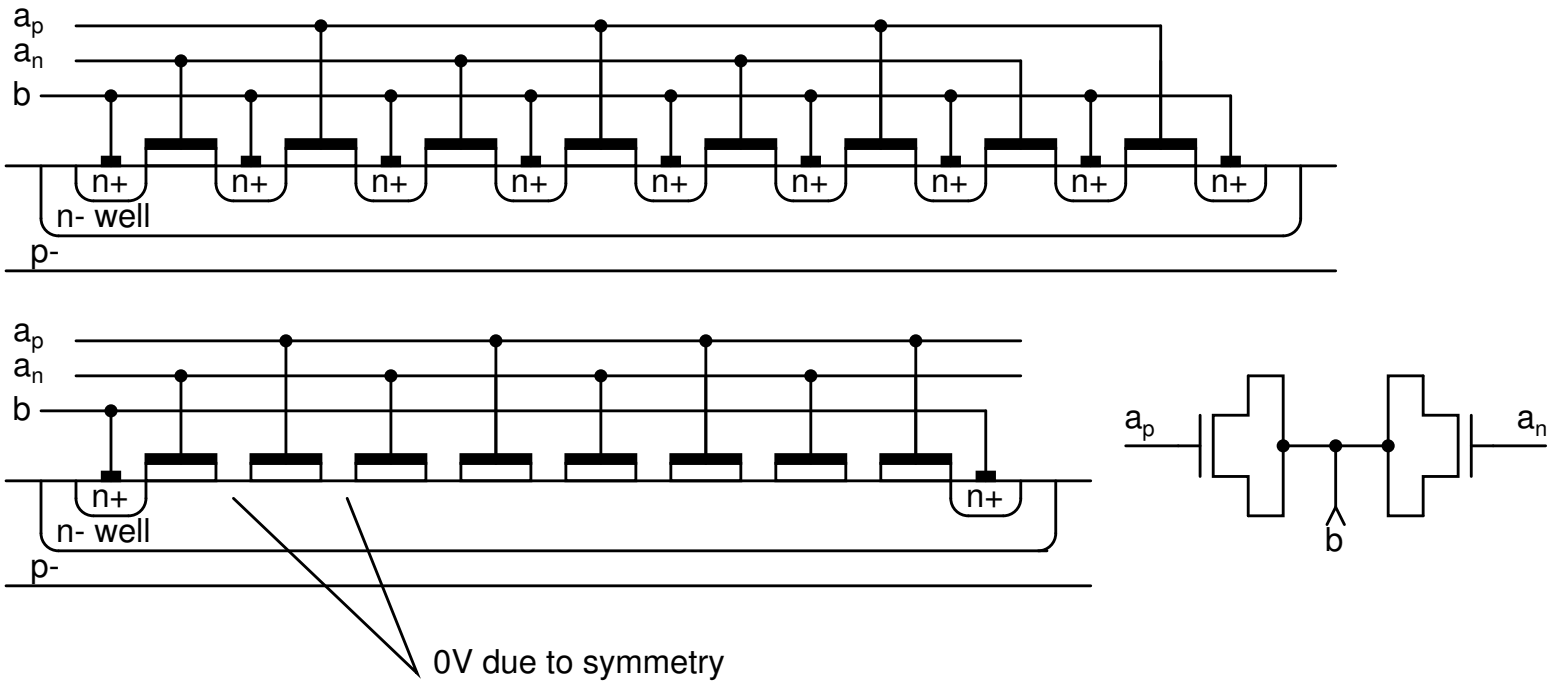
- Tunable using a varactor
- Reverse biased p-n junction
- MOS device in accumulation—larger tuning range; more popular in CMOS ICs

Accumulation MOS varactor



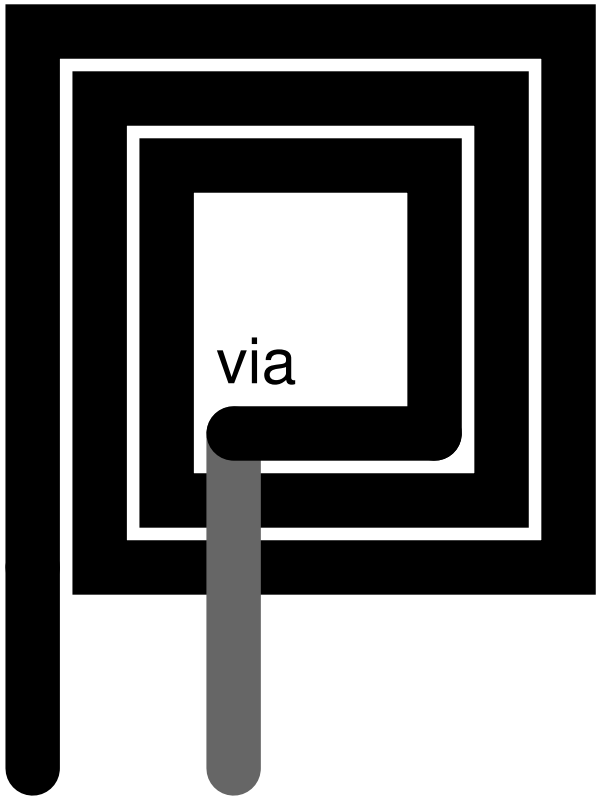
- nMOS in n-well
- Multi fingered structure to reduce gate, channel resistance
- $W \sim$ few microns; $L > L_{min}$ to reduce parasitics
- Gate contacts at both ends to further reduce resistance
- Quality factor: 20+

MOS varactor with differential excitation



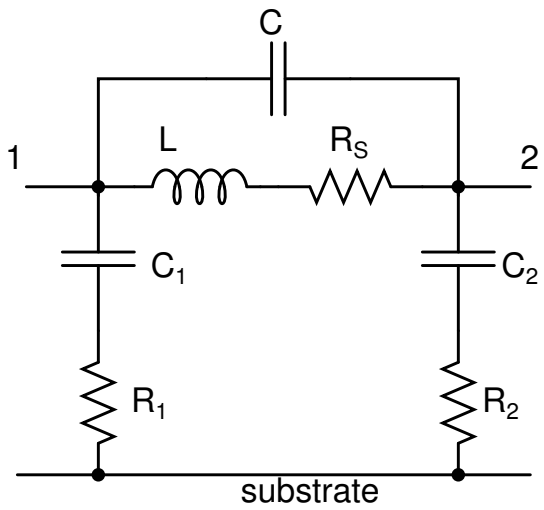
- Interdigitated fingers—alternate ones connected to a_p and a_n
- Region between gates connected to a_p and a_n at 0 V due to symmetry
- All n+ contacts except the ones at the end can be removed [7]
- Smaller structure, lower series resistance, and smaller parasitic capacitances

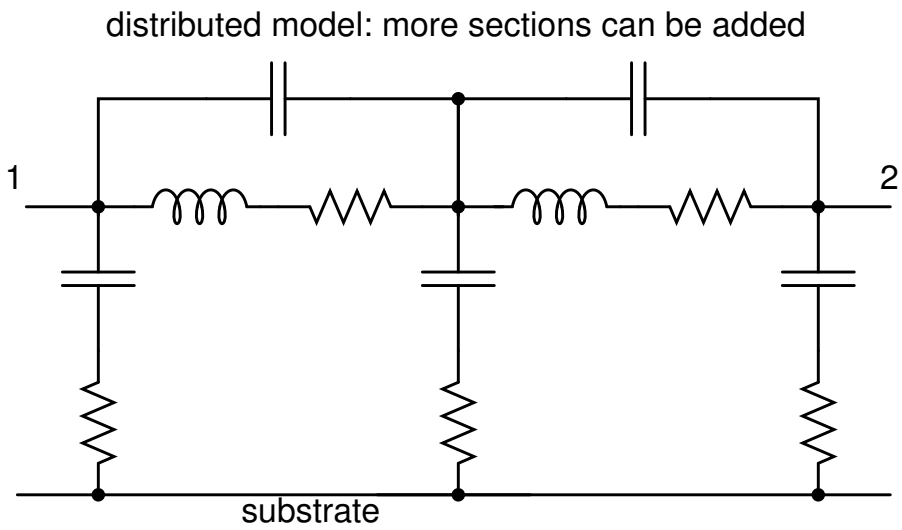
On chip inductors



- Planar inductor on one of the metal layers
- Top level metal preferred
  - Farther from the substrate
  - Smaller parasitic capacitance
  - Lesser coupling to substrate, and hence, loss
- Thicker top level metal ($\sim 2\,\mu$m) available in mixed signal processes

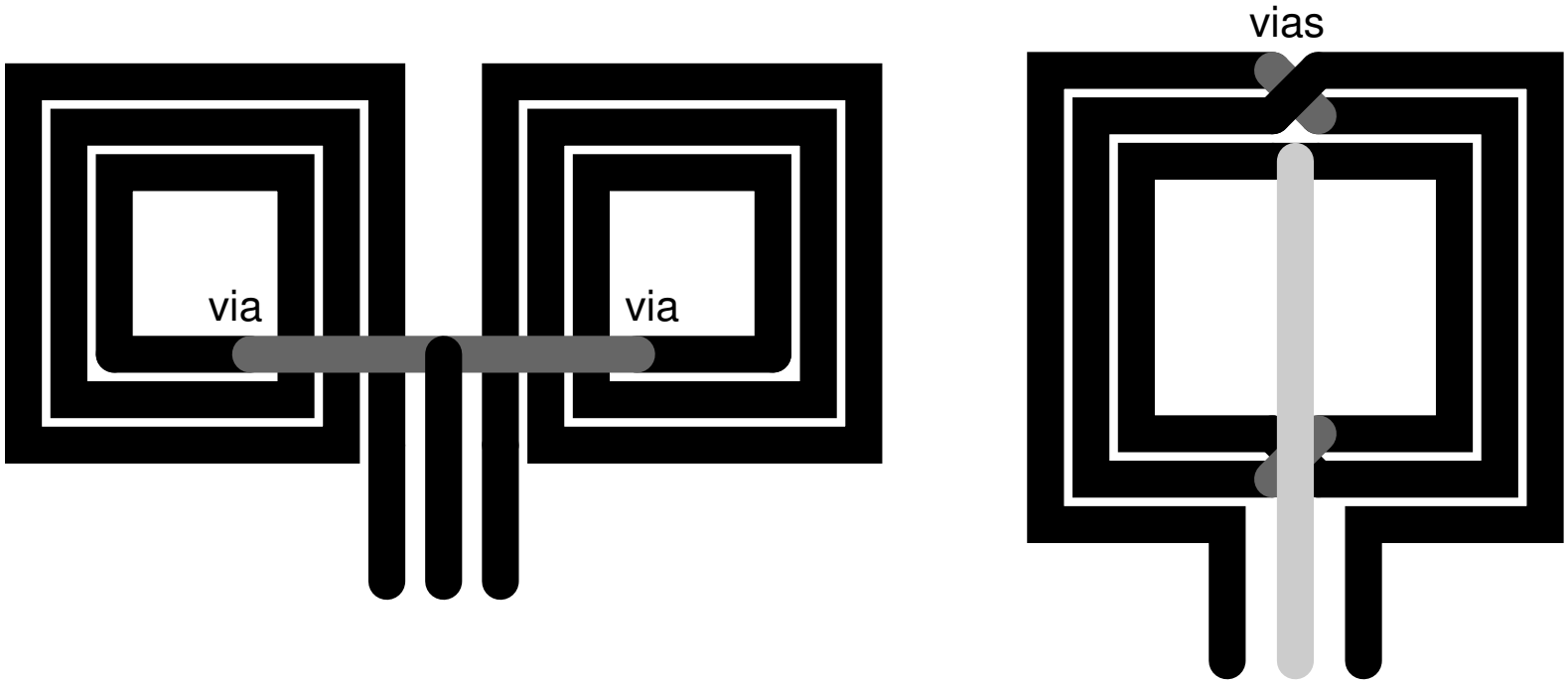
Inductor loss mechanisms





- Winding resistance
  - $R_\square L/W$
  - Effective $R_\square$ larger due to skin effect
  - Copper: 2 μm skin depth ($\propto 1/\sqrt{f}$) at 1 GHz
- Capacitive coupling to substrate and its resistance
- Inductive coupling to (resistive) substrate
- Quality factors upto 15 possible, typically 8-10
- Use adequate thickness and number of vias during layout

Differential inductor



- Symmetrical differential inductor
  - More compact for a given differential inductance
  - Larger potential difference between turns $\Rightarrow$ larger effect of interwinding parasitic capacitance
- Symmetrically laid out single ended inductors
  - Greater area
  - Interwinding parasitic capacitance not very significant

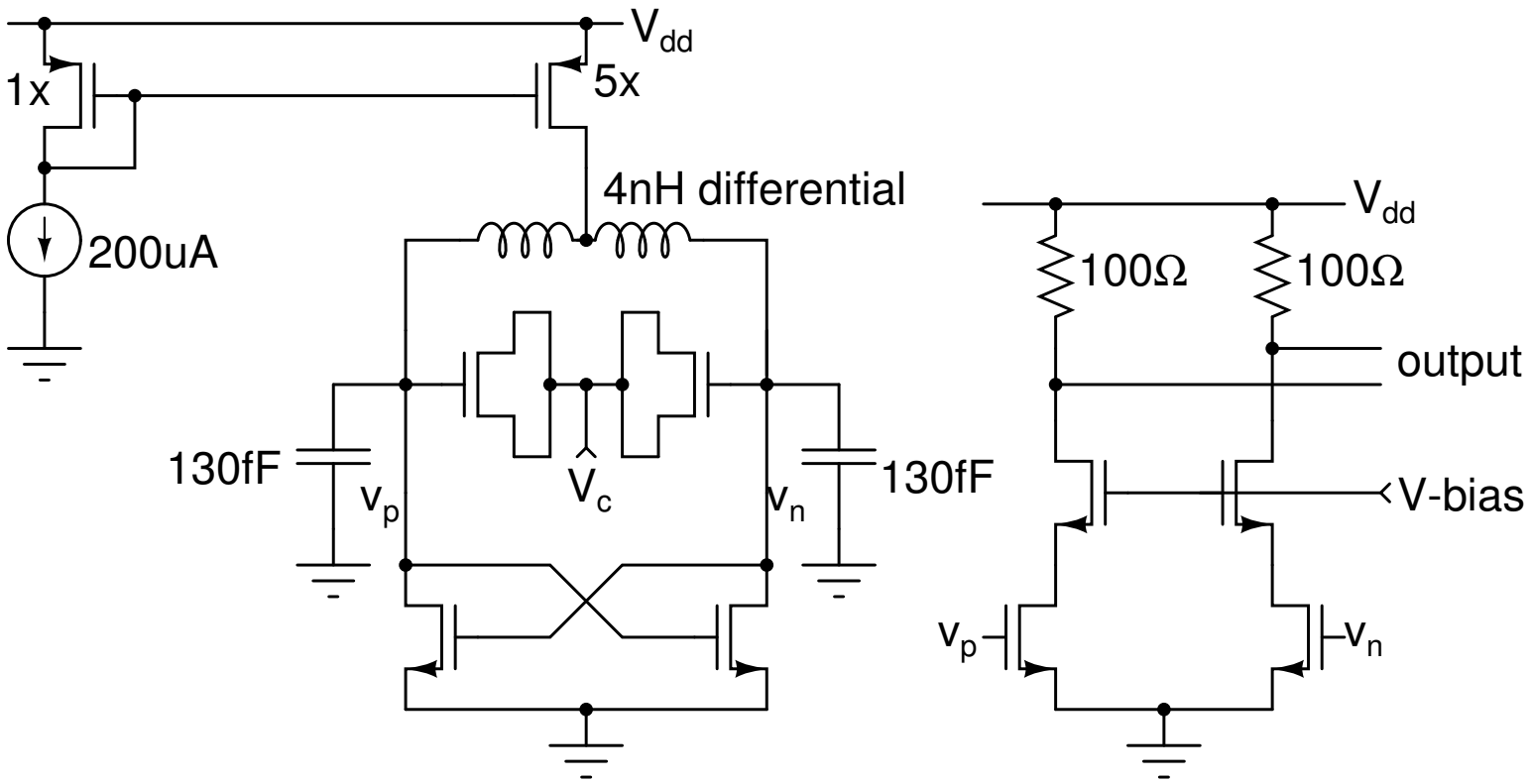
Inductor simulation

- Some processes have scalable inductor library and models
- Typically needs to be simulated from process parameters—metal thickness, resistivity, intermetal spacing etc.
- Inductance value
  - FastHenry, Asitic etc.
  - Accurate estimation possible
- Quality factor
  - FastHenry, Asitic etc.
  - Harder to accurately estimate losses due to substrate coupling
- Parasitic capacitance
  - First order parallel plate estimation—OK for single ended inductors
  - FastCap etc.
  - Use distributed models for accuracy—2 to 3 sections are sufficient

VCO design: bias current and transistor sizing

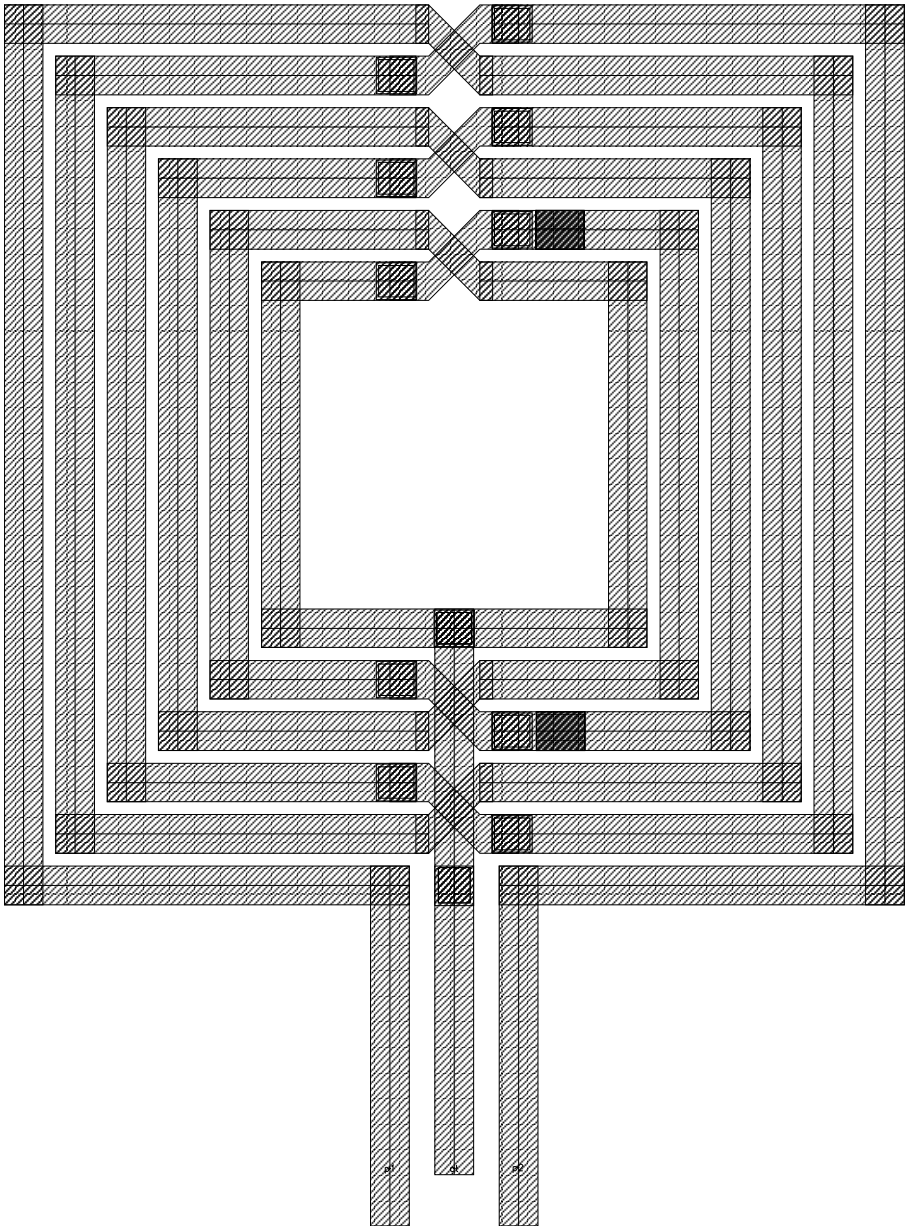
- Bias current is a function of tank losses and desired amplitude
  - Maximize the inductance for a large amplitude from a small current
- Transistors typically minimum length at high frequencies—longer to lower $1/f$ corner
- Bias source: longer than minimum length to lower $1/f$ noise
- Minimize all parasitics to maximize tuning range from the varactor
- Transistor W/L to get the desired g_m for startup in the worst case
  - Large $g_m \Rightarrow$ increased phase noise; So don't go crazy!
  - Minimize g_m variations over process and temperature; Less overdesign

5 GHz VCO in 0.18 μm CMOS

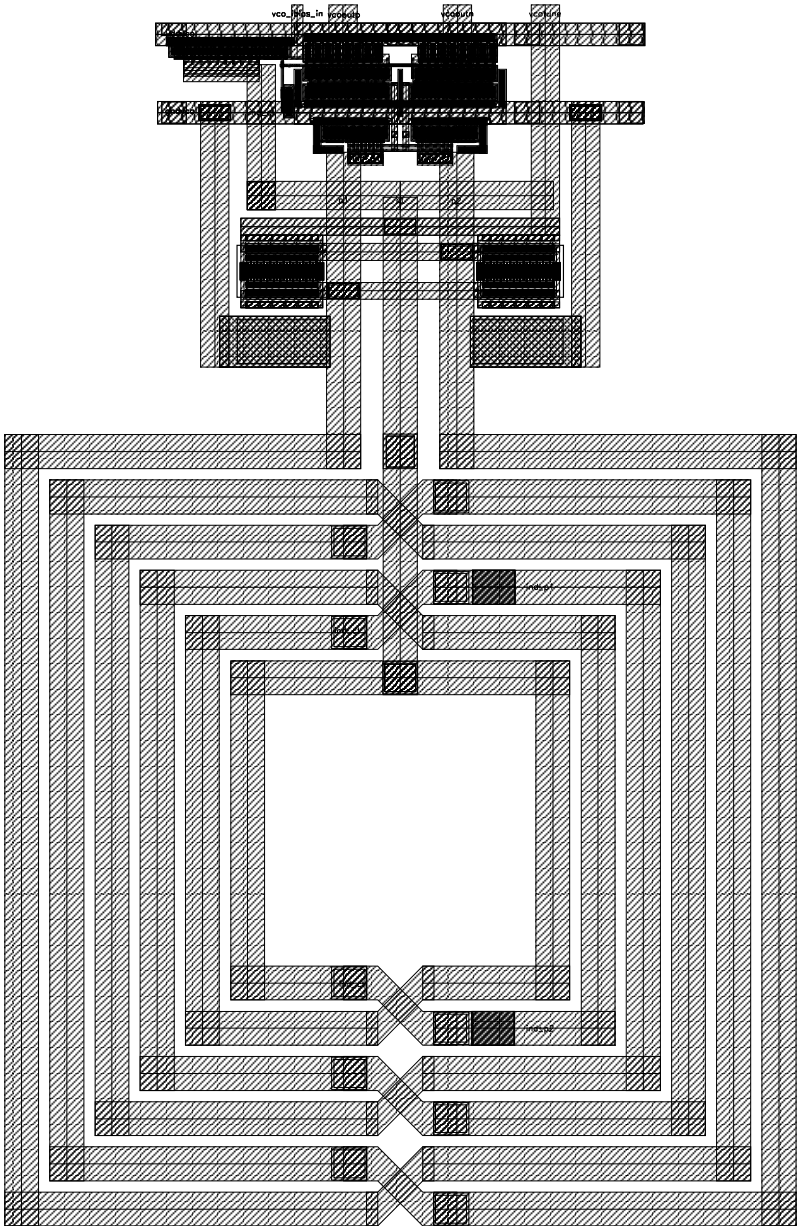


- $L = 4$ nH and $C = 0.25$ pF (differential) chosen
- 6 turn inductor on top metal layer, $\approx 140\,\mu$m square
- From inductor simulations, $Q \approx 6$
- Minimum length transistors
- Cascode buffer for measurement

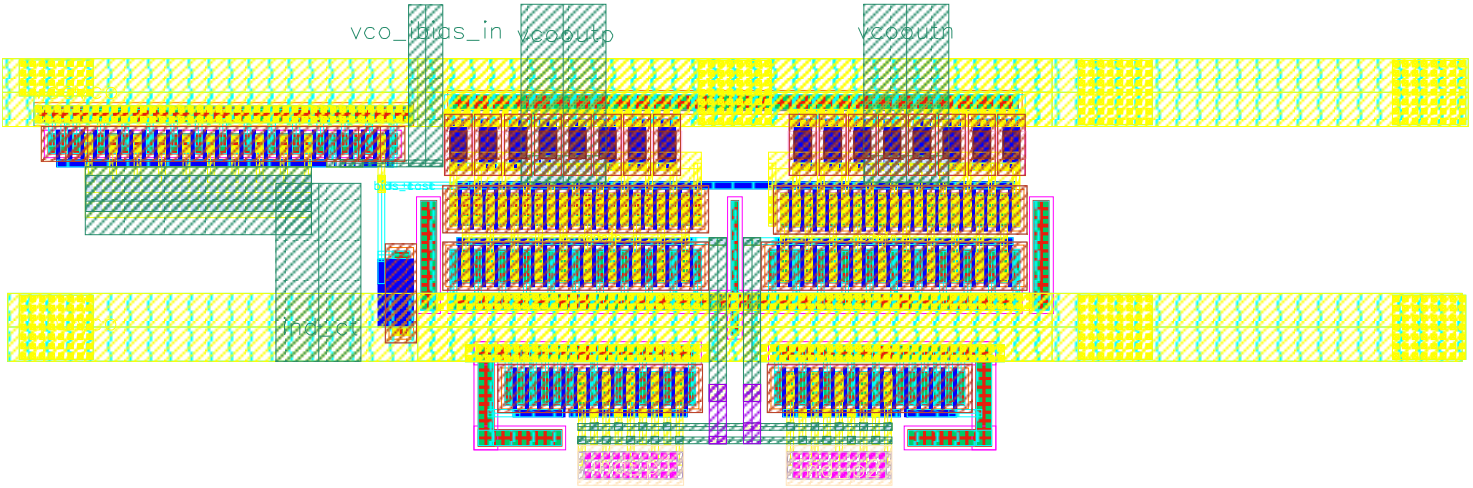
5GHz VCO-inductor



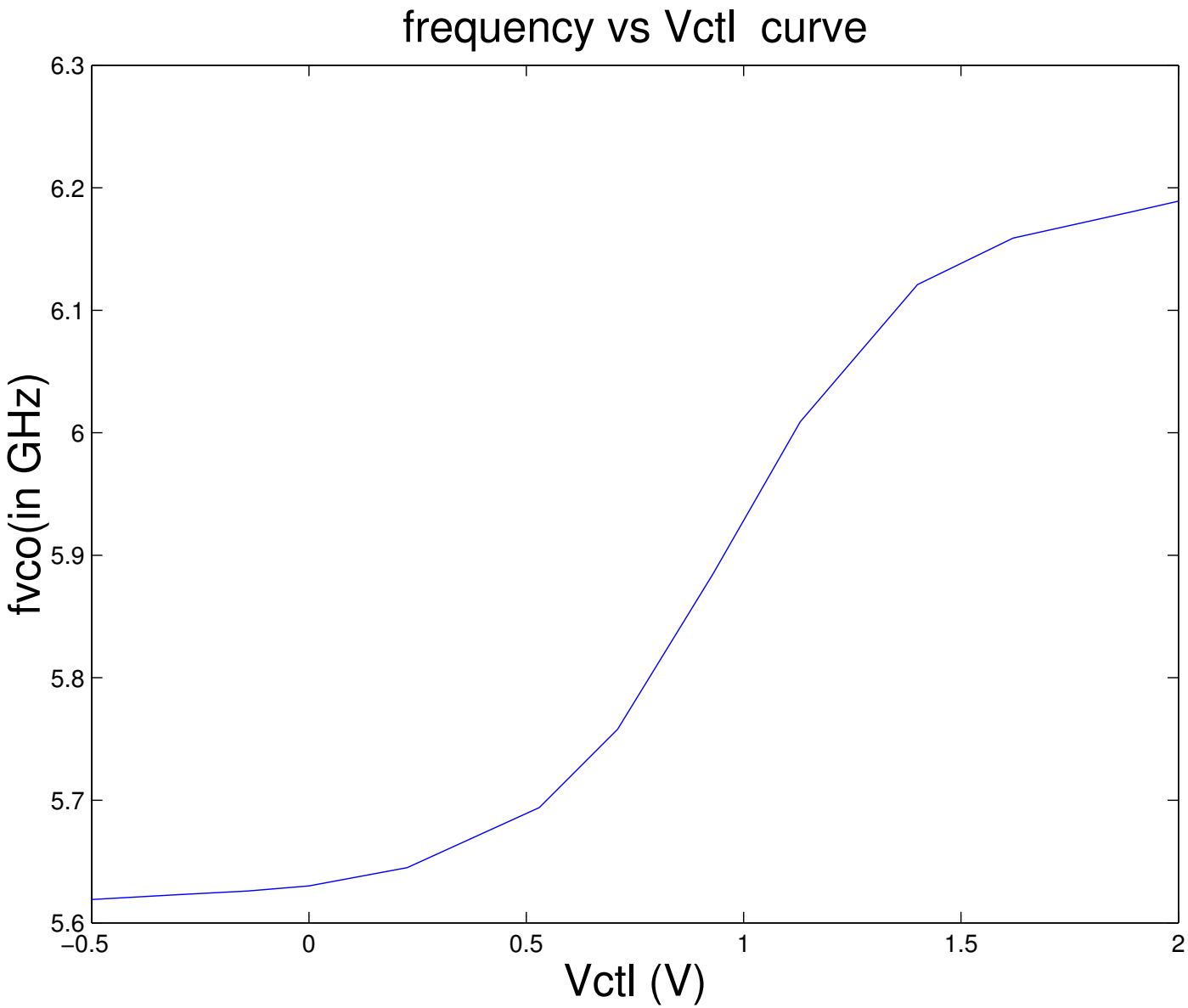
5GHz VCO layout



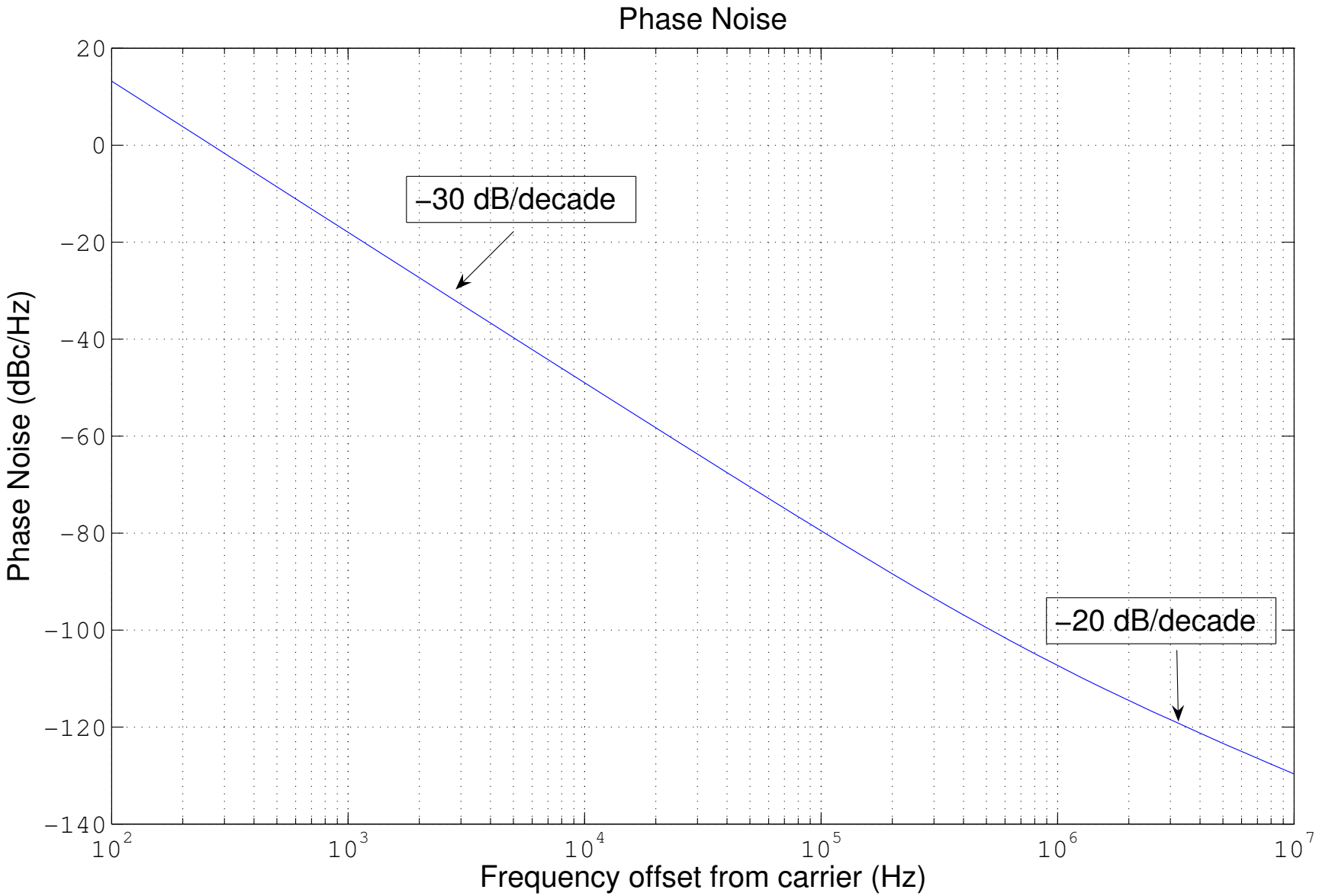
5GHz VCO layout



VCO (higher freq. version)-measured f vs. V

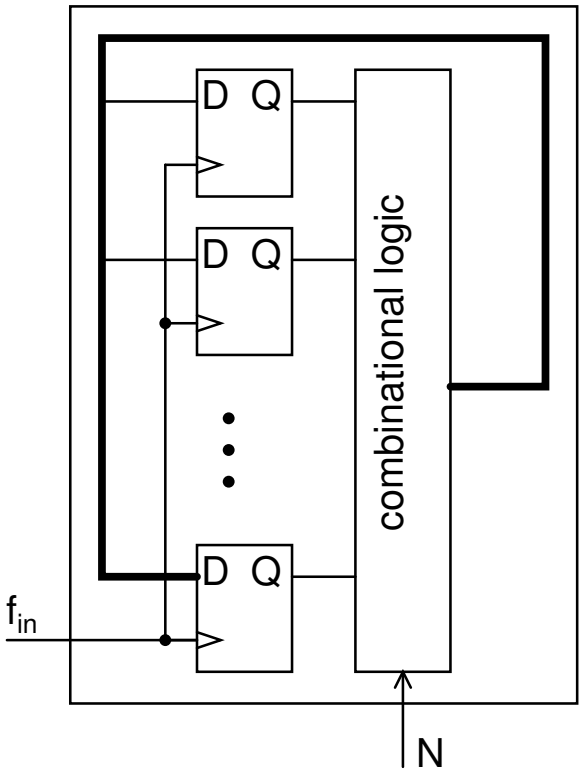


VCO-simulated phase noise



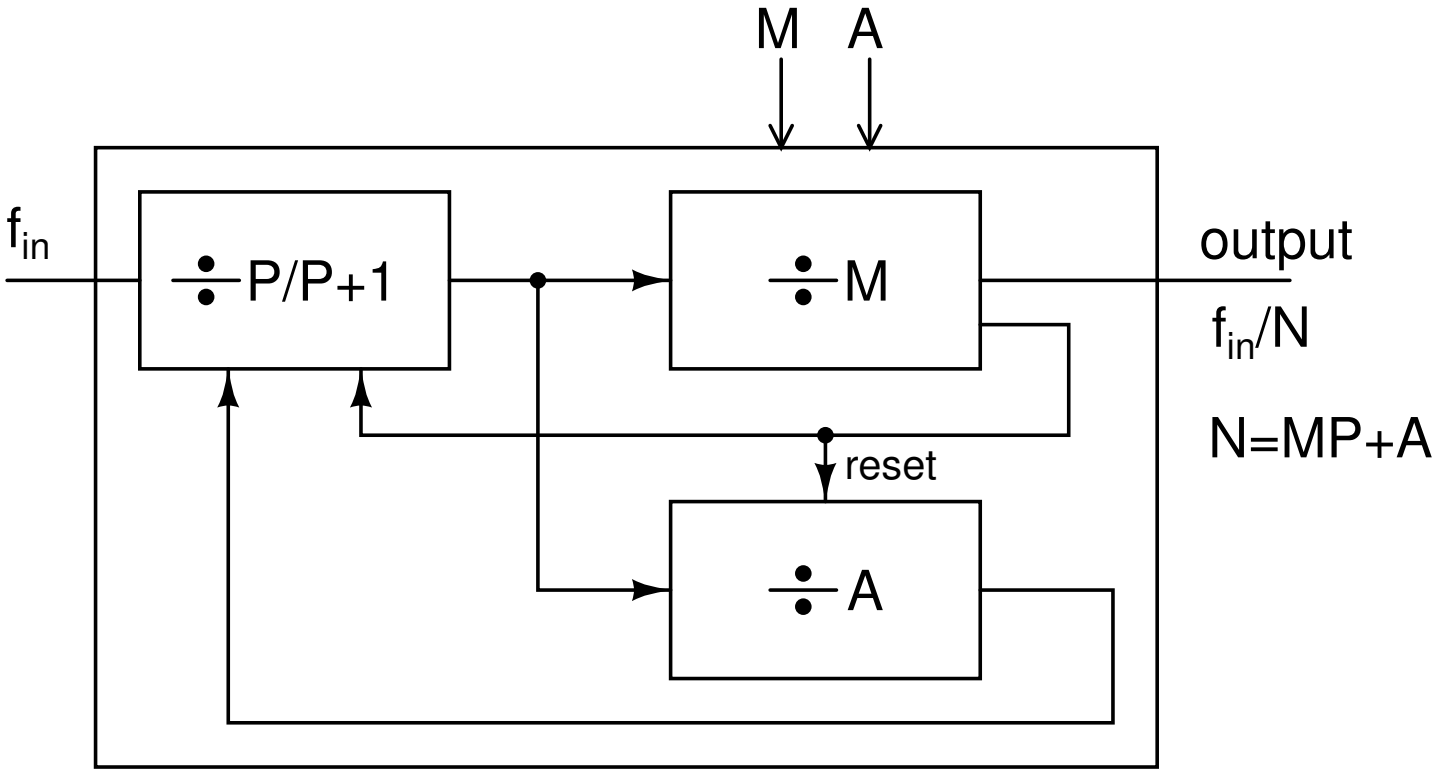
Programmable frequency divider

Programmable divider-Synchronous counter



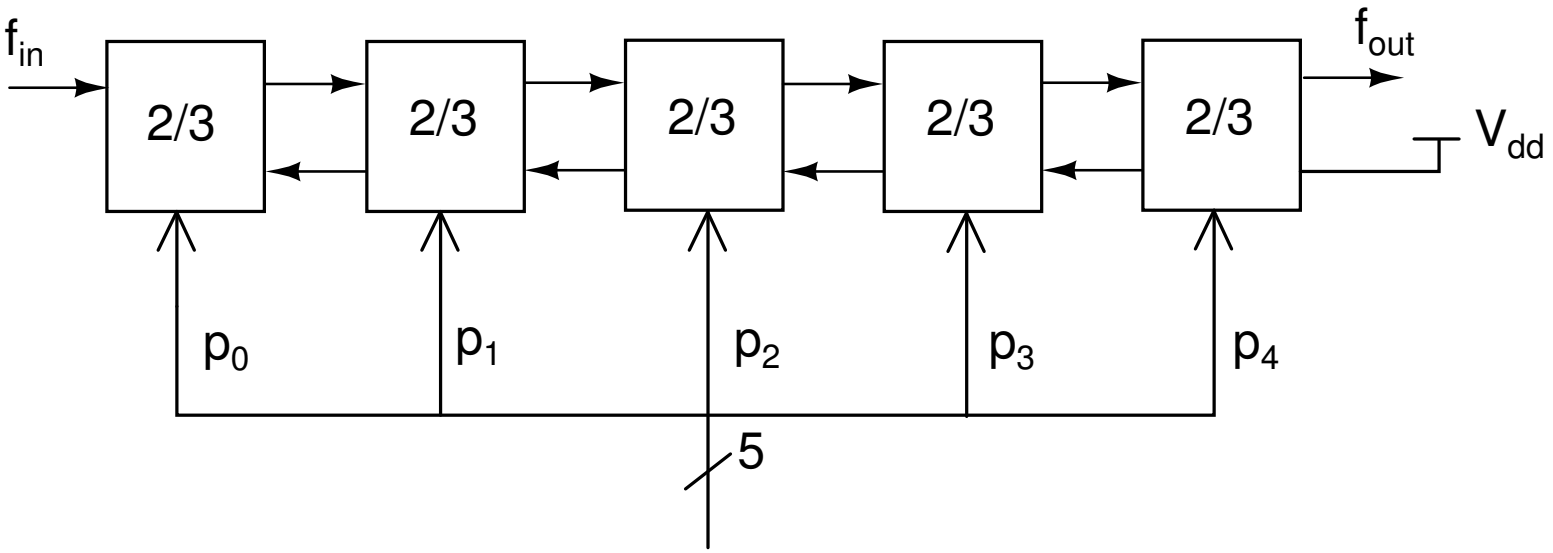
- All of the circuitry running at full speed
- Very high power dissipation
- Asynchronous operation preferred

Programmable divider-Pulse swallow architecture



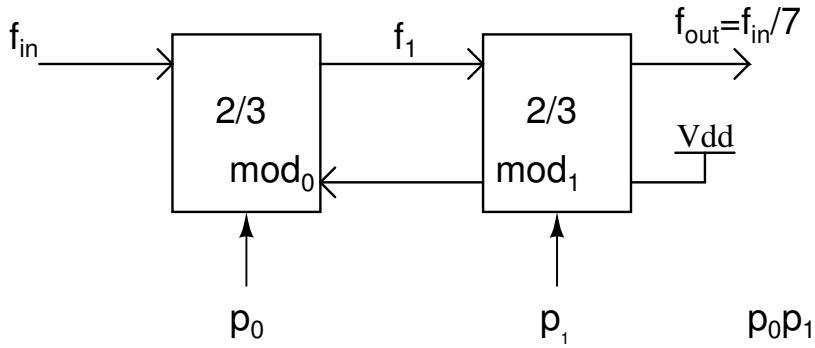
- Dual modulus prescaler $\div P/P+1$
- Divide by $P+1$ for A cycles
- Divide by P for $M-A$ cycles
- Full cycle = $(P+1)A + P(M-A) = MP + A$
- Only the dual modulus prescaler running at full speed
- Programmability using M and A

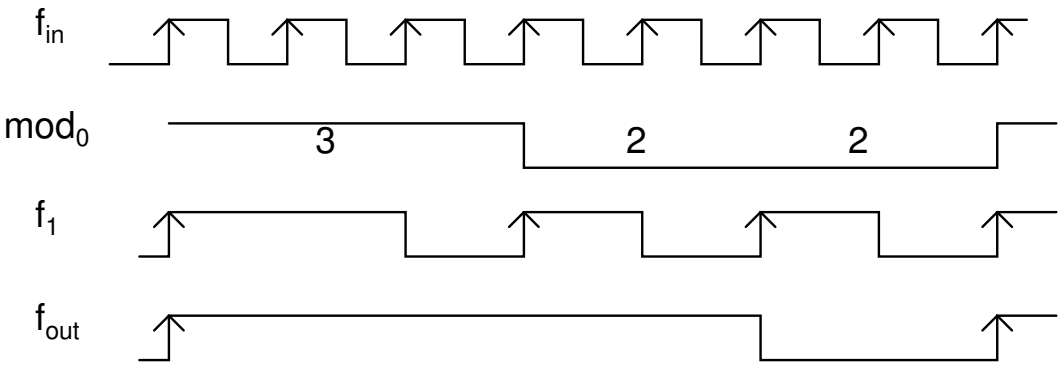
Programmable divider using divide-by-2/3 cells



- Each stage divides by 2 (if $p_k = 0$)
- Each stage divides by 3 (if $p_k = 1$) once in each output cycle
- With L stages, the division factor range from 2^L to $2^{L+1} - 1$
- Modular approach

Programmable divider using divide-by-2/3 cells





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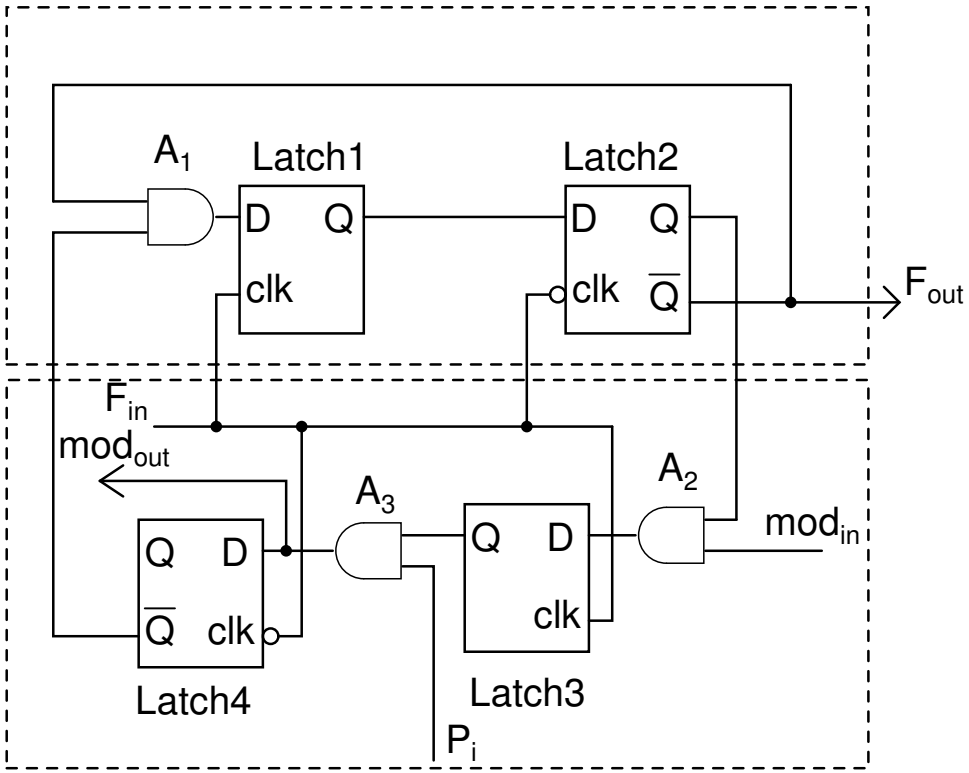
- Modular approach

Divide-by-2/3 cell for the programmable divider



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