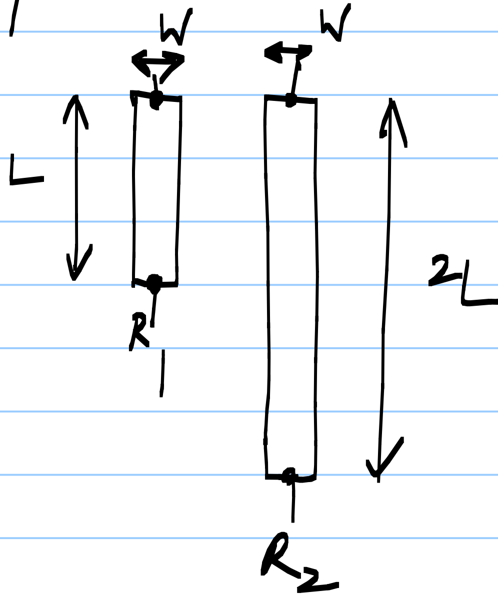
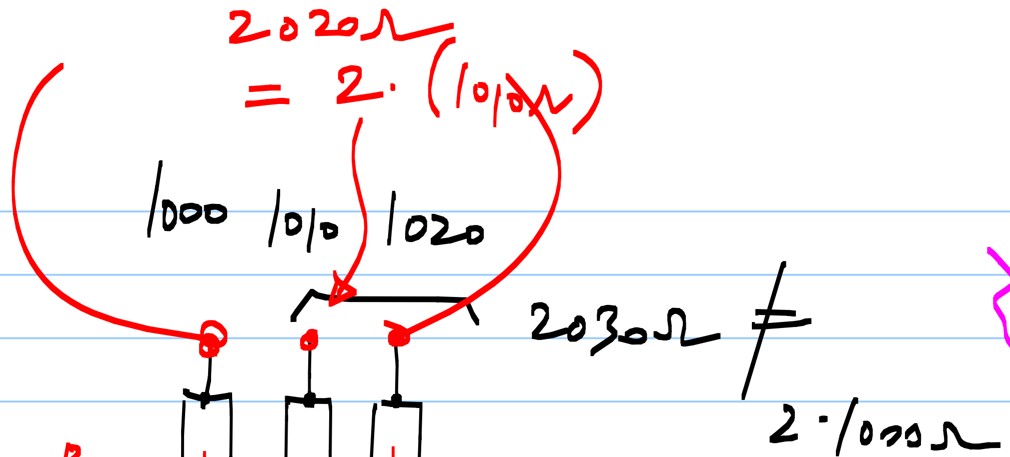
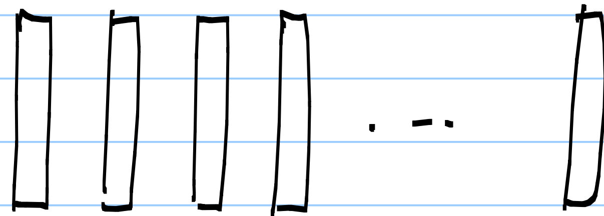
$$\frac{R_2}{R_1} = 2$$







R R+ΔR R+2ΔR - - -

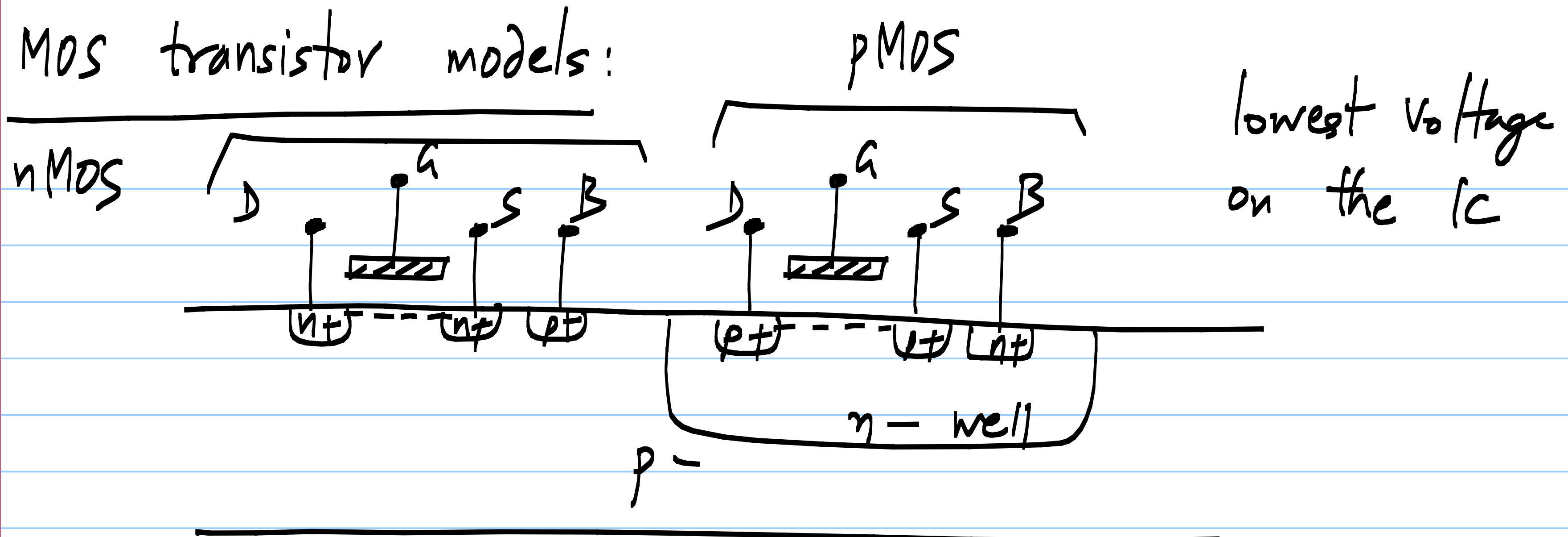
Lecture 21

* Resistors, capacitors: Large variation in absolute value (process variations)
* Physically identical components – closely matched values
* Relative mismatch: $\sigma\left(\frac{\Delta R}{R_0}\right) = \sigma_R = \frac{A_R}{\sqrt{WL}}$

$$\sigma\left(\frac{\Delta C}{C_0}\right) = \sigma_C = \frac{A_C}{\sqrt{WL}}$$

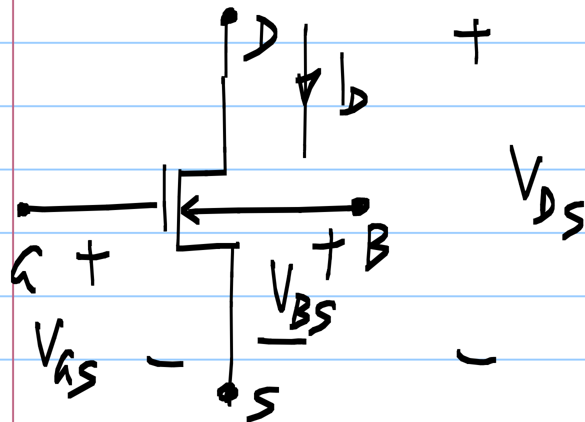
* Identical layout environment – good matching
  – dummy devices, common centroid.

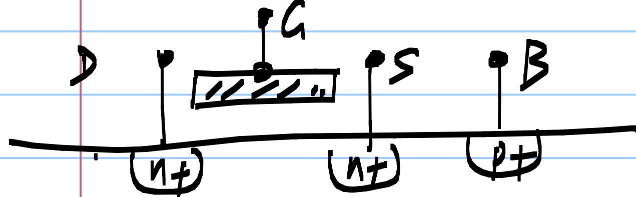
MOS transistor models:



* nMOS bulk (substrate) — lowest voltage on the IC
* triple well process — nMOS transistors with isolated bulk nodes
* pMOS transistor is formed inside an n− well

MOS transistor large signal model





p−

$V_{DS} > 0$

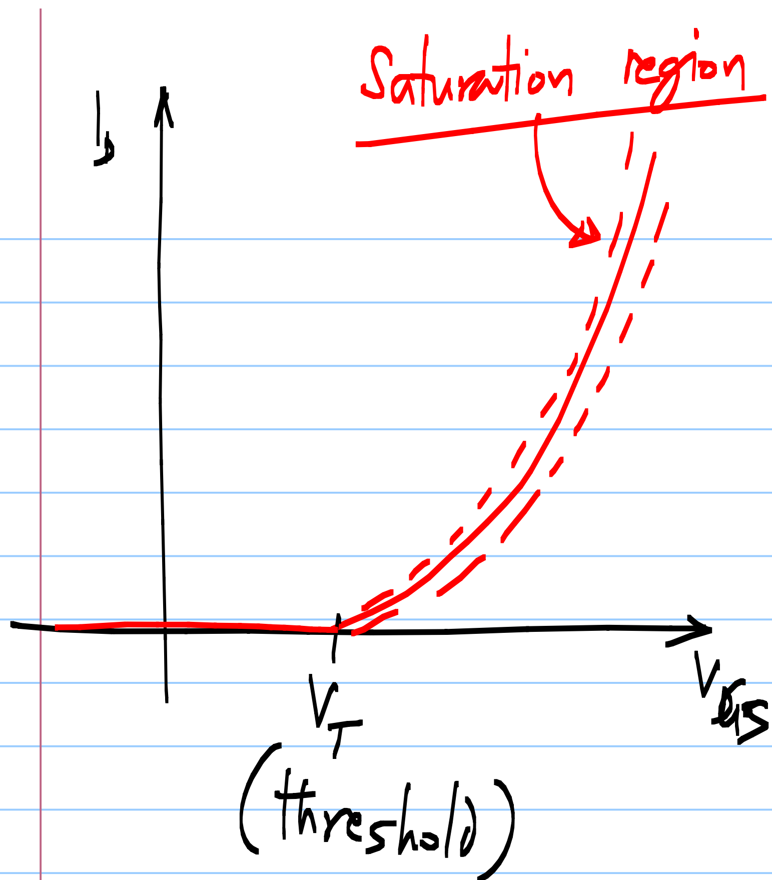
$$I_D = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

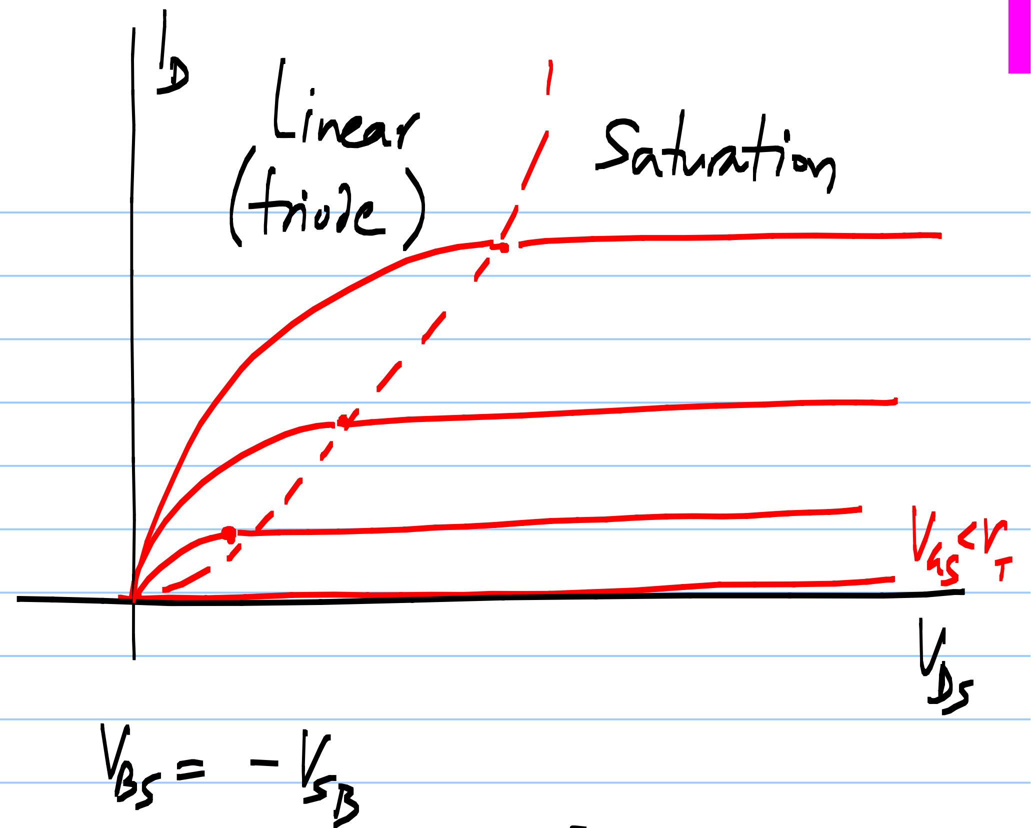
[Saturation region] $V_{GS} > V_T$, $V_{DS} > V_{GS} - V_T$

$$= \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

[linear triode] $V_{GS} > V_T$, $V_{DS} < V_{GS} - V_T$

$$= 0$$ [cutoff] $V_{GS} < V_T$

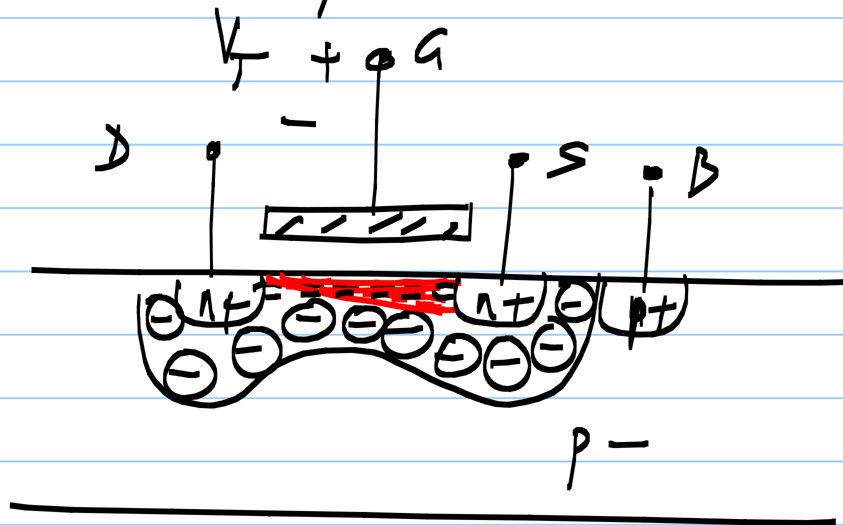




$V_{BS} = -V_{SB}$

Threshold voltage $V_T = V_T(V_{SB}) = V_{T0} + \gamma \left[\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F} \right]$

(1) saturation / triode boundary :



$V_{DS} > V_{GS} - V_T$

$V_D > V_G - V_T$

$(V_G - V_D) < V_T$

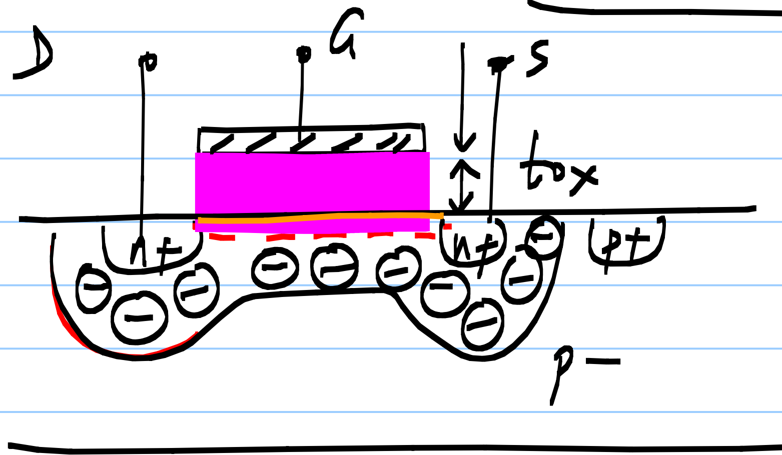
* $V_T = V_{GD} (= V_{GS})$ required to form the inversion layer.

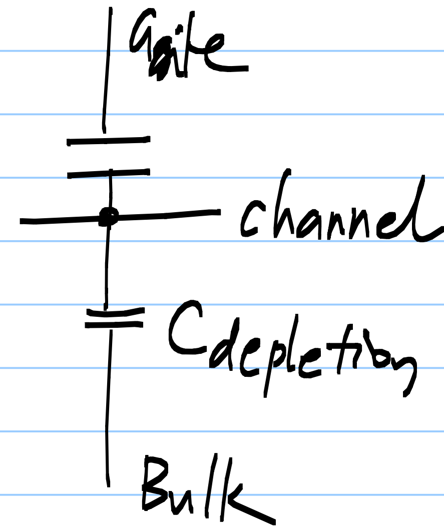
* $V_D > V_S \Rightarrow$ More inversion at the source end compared to the drain end.

Saturation: drain end not inverted

(ii) Effect of V_{SB}:

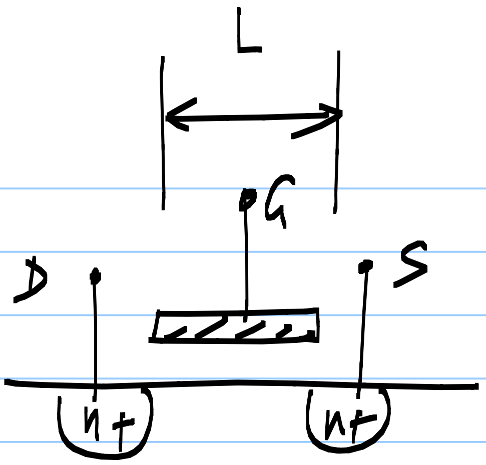
$$C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

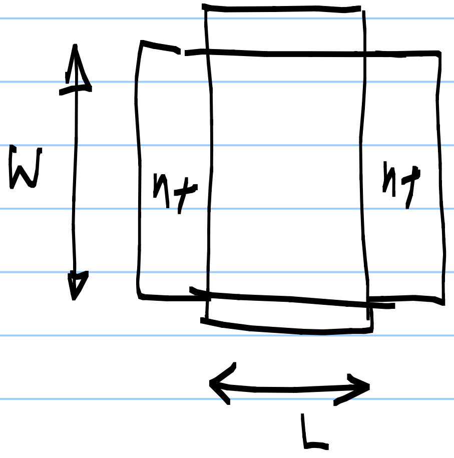




* Increase the gate or bulk voltage — channel charge & the drain current tend to increase

bulk —— back gate


L
G
D
S
n+
n+


W
n+
n+
L

Increasing either V_{GS} or V_{BS} increases the current

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} \left(V_{GS} - V_T\right)^2 \left(1 + \lambda V_{DS}\right)$$

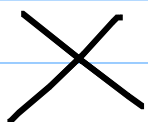
[Saturation]

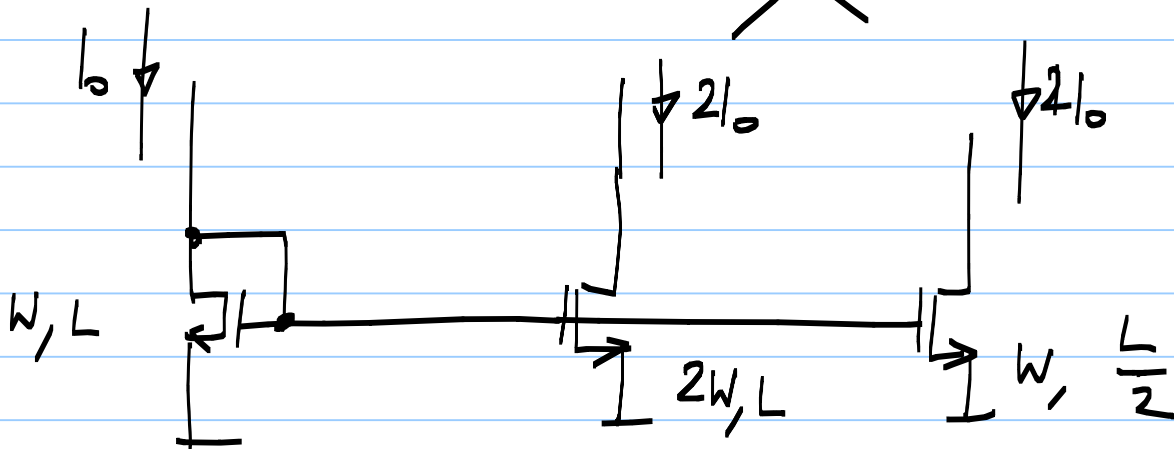
$$V_T = V_{T0} + \gamma\left(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right)$$

Body effect

$$I_D = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

$$I_D \propto W \; ; \quad I_D \propto \frac{1}{L}$$

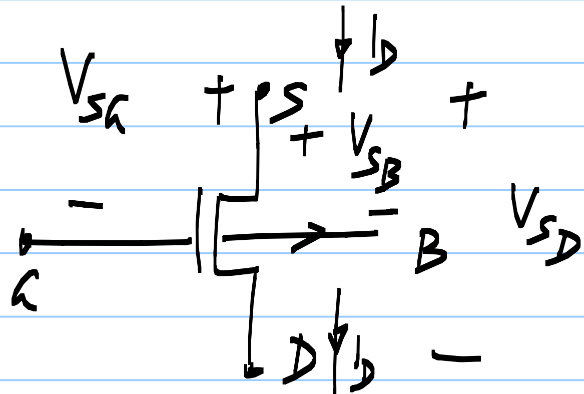


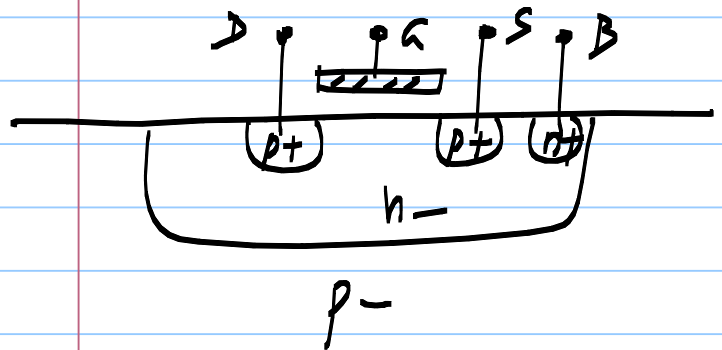


Use ratio of widths for multiplying currents;

Do not use ratio of lengths

pMOS transistor:





$$I_D = \frac{\mu_p C_{ox}}{2} \frac{W}{L} (V_{SG} - V_{Tp})^2$$

$V_{SD} > V_{SG} - V_{Tp}$; $V_{SG} > V_{Tp}$

(saturation region)

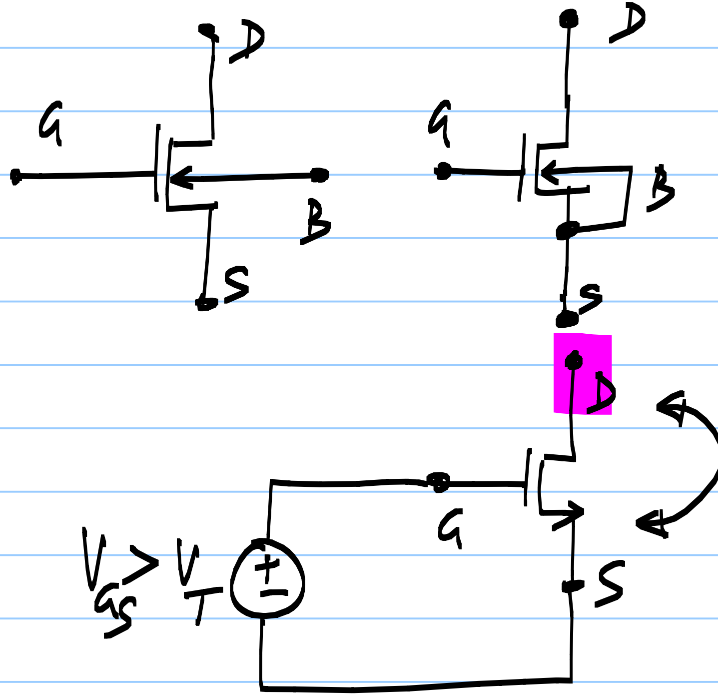
triode $\mu_p C_{ox} \frac{W}{L} \left[(V_{SG} - V_{Tp}) \cdot V_{SD} - \frac{V_{SD}^2}{2} \right]$

$V_{SD} < V_{SG} - V_{Tp}$; $V_{SG} > V_{Tp}$

cutoff 0 ; $V_{SG} < V_{Tp}$

$$V_{Tp} = V_{T0} + \gamma \left(\sqrt{V_{BS} + 2\phi_F} - \sqrt{2\phi_F} \right)$$

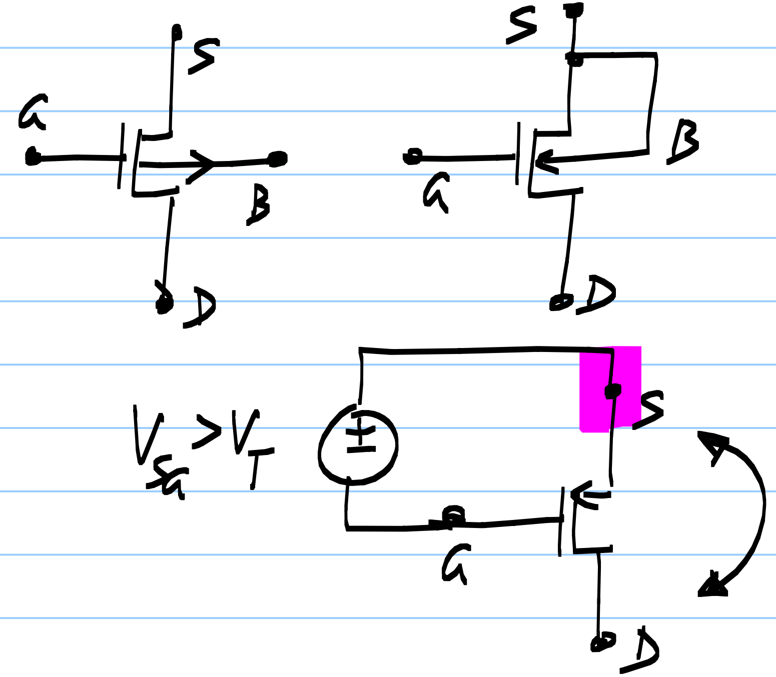
nMOS.



$$V_{DS} > V_{GS} - V_T$$

$$V_D > V_G - V_T$$

pMOS



$$V_{SD} > V_{SG} - V_T$$

$$+V_D < +V_G + V_T$$

Subthreshold operation:

Square law

$V_{GS} > V_T$; $V_{SG} > V_T$: strong inversion
(nMOS) (pMOS)

$V_{GS} < V_T$: non zero current

$$I_D = I_0 \cdot \exp\left(\frac{V_{GS}}{\eta V_t}\right)$$

$I_0 \propto W$

Exponential device

$$V_t = \frac{kT}{q} = 25.9 \text{ mV @ } 300K$$

thermal voltage