

## References

- 1 B. A. Minch, C. Diorio, P. Hasler, and C. A. Mead, "Translinear Circuits Using Subthreshold Floating-Gate MOS Transistors," *J. Analog Integrated Circuits Signal Process.*
- 2 X. Arreguit, E. A. Vittoz, F. A. van Schaik, and A. Mortara, "Analog Implementation of Low-Level Vision Systems," in *Proceedings of European Conference on Circuit Theory and Design*, Elsevier, 1993, pp. 275-280.
- 3 M. H. Cohen and A. G. Andreou, "Analog CMOS Integration and Experimentation with an Autoadaptive Independent Component Analyzer," *IEEE Trans. Circuits Systems: Part II: Analog Digital Signal Proc.*, vol. 42, no. 2, pp. 65-77, 1995.
- 4 B. L. Hart, "Translinear Circuit Principle: A Reformulation," *Electronic Letters*, vol. 15, no. 24, pp. 801-803, 1979.
- 5 V. De, S. Borkar, "Technology and Design Challenges for Low Power and High Performance," in *Proceedings of International Symposium on Low Power Electronics and Design*, pp. 163-168, August 1999.
- 6 A. Keshavarzi, K. Roy, and C. F. Hawkins, "Intrinsic Leakage In Low Power Deep Submicron CMOS Ics," in *Proceedings of International Test Conference*, pp. 146-155, 1997.
- 7 J. Brews, *High Speed Semiconductor Devices*, S. M. Sze, New York, USA: John Wiley & Sons, 1990, ch. 3.
- 8 Y. Tsividis, *Operation and Modeling of the MOS Transistor*, McGraw-Hill, New York, 1987.
- 9 R. H. Dennard, F. H. Gaenslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. R. LeBlanc, "Design Of Ion-Implanted Mosfets With Very Small Physical Dimensions," *IEEE Journal of Solid-State Circuits*, SC-9, 256, 1974.
- 10 V. De et. al., "Techniques for Leakage Power Reduction," in *Design of High-Performance Microprocessor Circuits*, ed. A. Chandrakasan, W. J. Bowhill, and F. Fox, IEEE Press, Piscataway NJ, 2000, 46-62.