Overview

- Each processor in the 80x86 family has a corresponding coprocessor with which it is compatible
- Math Coprocessor is known as NPX,NDP,FUP.

  Numeric processor extension (NPX),

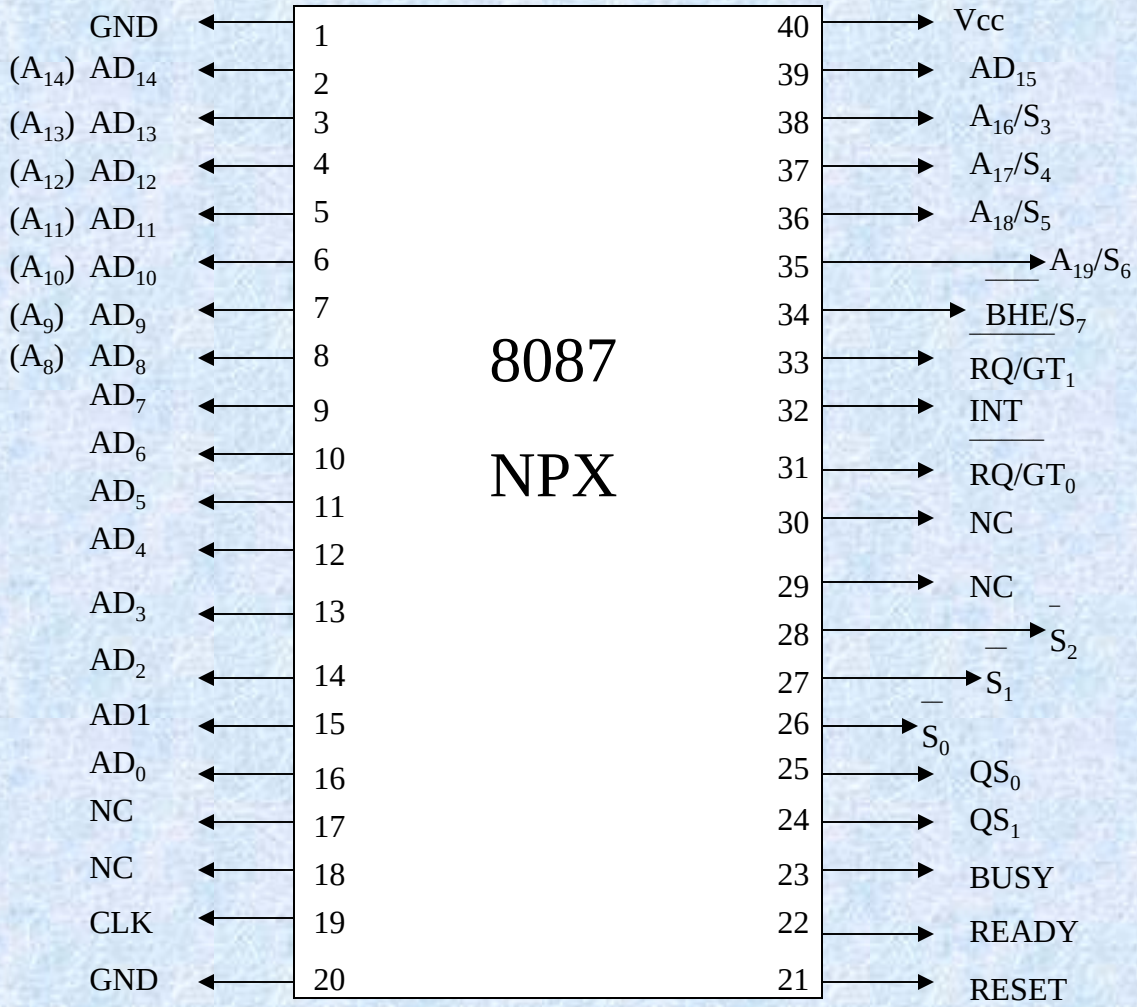
  Numeric data processor (NDP),

  Floating point unit (FUP).

Compatible Processor and Coprocessor

Processors	Coprocessors
1. 8086 & 8088	1. 8087
2. 80286	2. 80287,80287XL
3. 80386DX	3. 80287,80387DX
4. 80386SX	4. 80387SX
5. 80486DX	5. It is Inbuilt
6. 80486SX	6. 80487SX

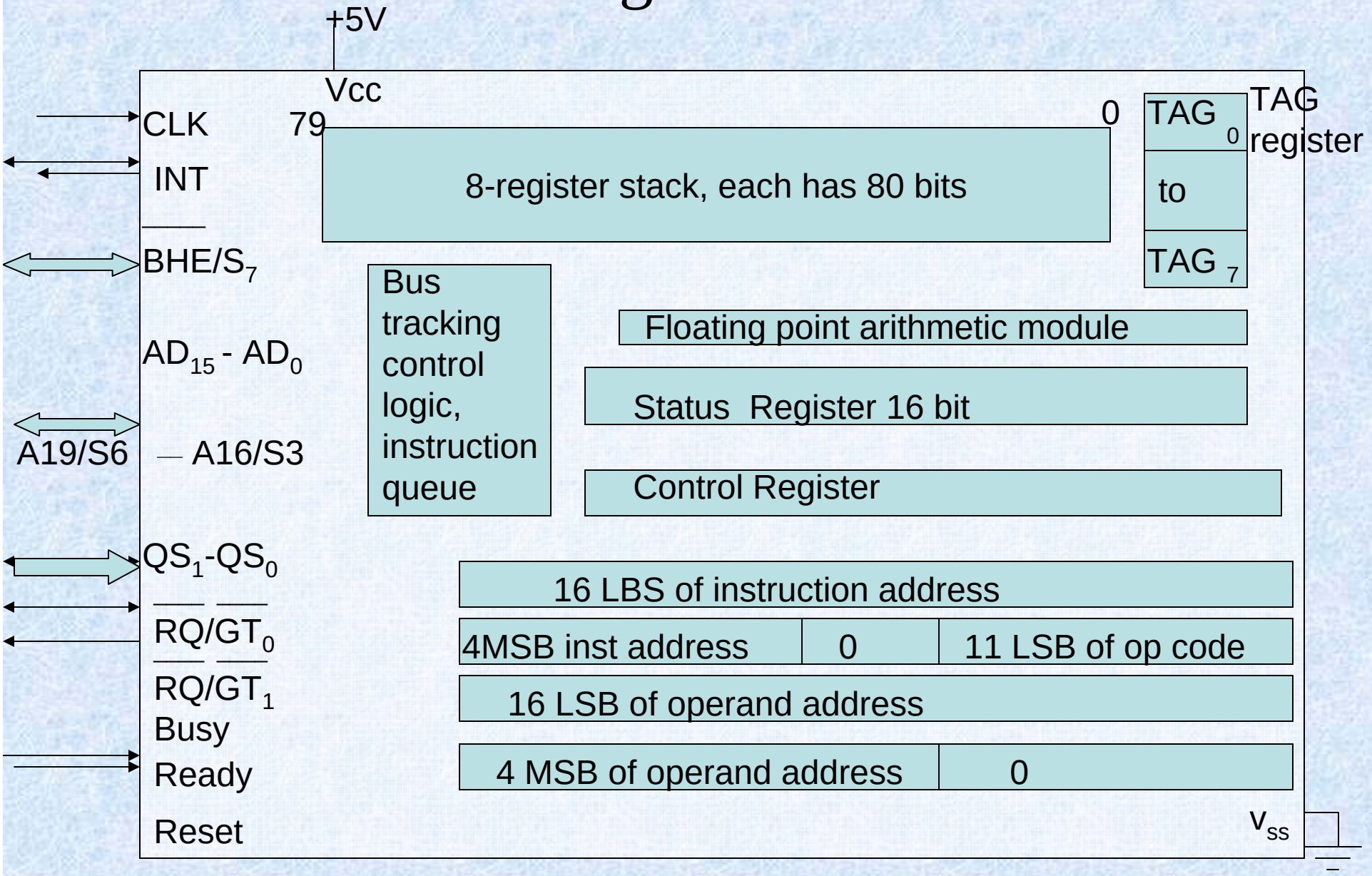
Pin Diagram of 8087



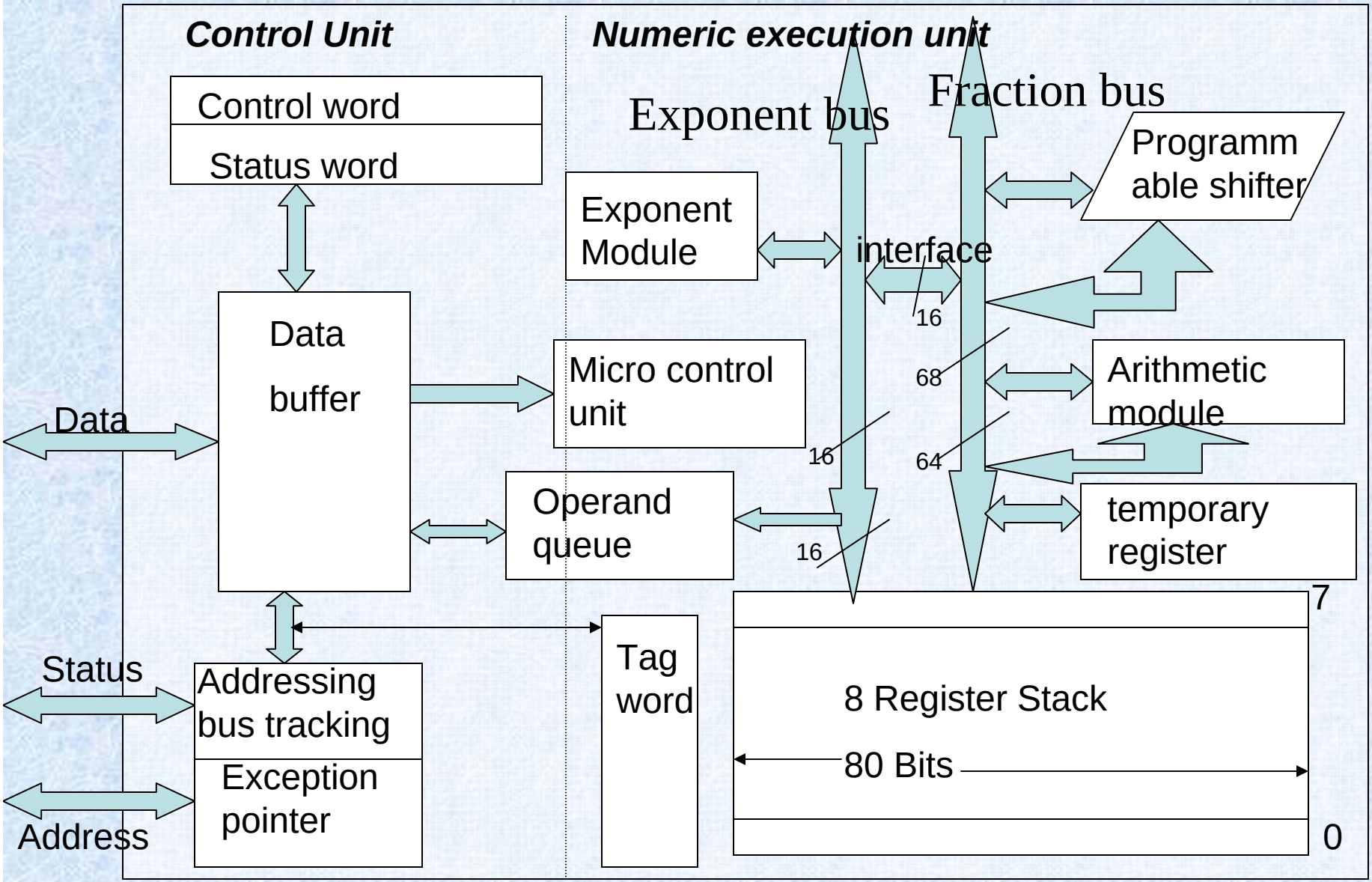
Architecture of 8087

- Control Unit
- Execution Unit

Block Diagram of 8087



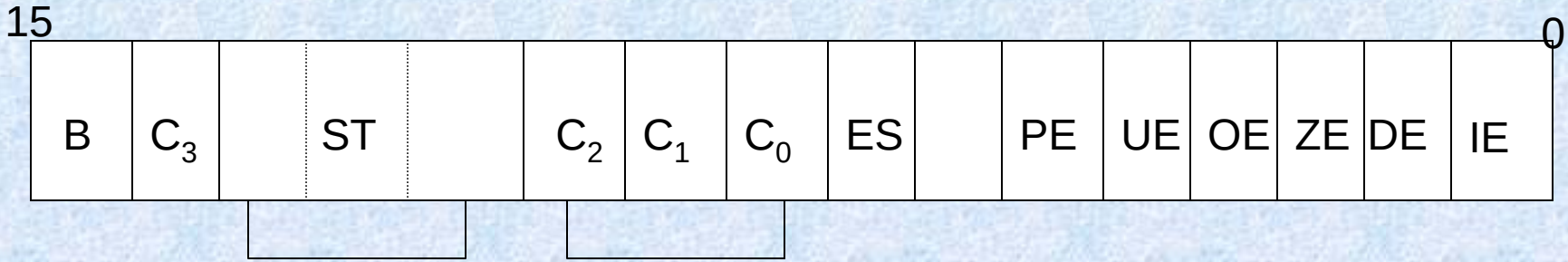
Block Diagram of 8087



Control Unit

- Control unit: To synchronize the operation of the coprocessor and the processor.
- This unit has a Control word and Status word and Data Buffer
- If instruction is an *ESC*ape (coprocessor) instruction, the coprocessor executes it, if not the microprocessor executes.

Status Register (cont..)



- C_3-C_0 Condition code bits
- TOP Top-of-stack (ST)
- ES Error summary
- PE Precision error
- UE Under flow error
- OE Overflow error
- ZE Zero error
- DE Denormalized error
- IE Invalid error
- B Busy bit

Status Register (cont..)

- Status register reflects the over all operation of the coprocessor.
- B-Busy bit indicates that coprocessor is busy executing a task. Busy can be tested by examining the status or by using the FWAIT instruction. Newer coprocessor automatically synchronize with the microprocessor, so busy flag need not be tested before performing additional coprocessor tasks.
- C_3-C_0 Condition code bits indicates conditions about the coprocessor.

Status Register (cont..)

- TOP- Top of the stack (ST) bit indicates the current register address as the top of the stack.
- ES-Error summary bit is set if any unmasked error bit (PE, UE, OE, ZE, DE, or IE) is set. In the 8087 the error summary is also caused a coprocessor interrupt.
- PE- Precision error indicates that the result or operand executes selected precision.
- UE-Under flow error indicates the result is too large to be represent with the current precision selected by the control word.

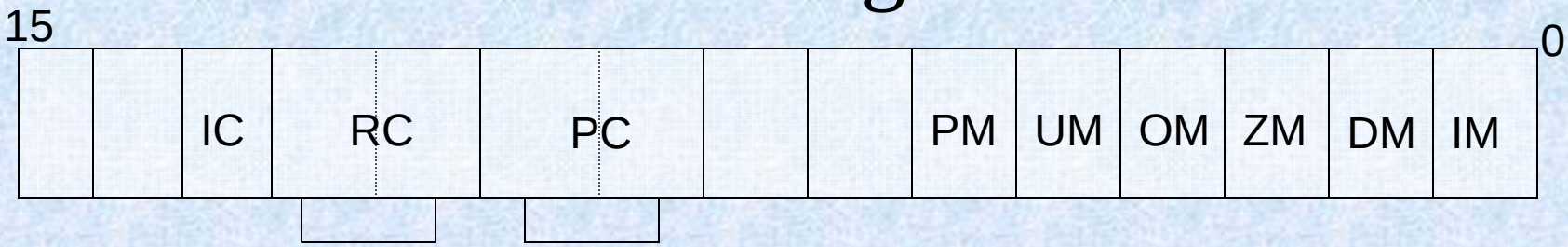
Status Register (contd..)

- OE-Over flow error indicates a result that is too large to be represented. If this error is masked, the coprocessor generates infinity for an overflow error.
- ZE-A Zero error indicates the divisor was zero while the dividend is a non-infinity or non-zero number.
- DE-Denormalized error indicates at least one of the operand is denormalized.
- IE-Invalid error indicates a stack overflow or underflow, indeterminate from (0/0,0,-0, etc) or the use of a NAN as an operand. This flag indicates error such as those produced by taking the square root of a negative number.

Control Register

- Control register selects precision, rounding control, infinity control.
- It also masks an unmasks the exception bits that correspond to the rightmost Six bits of status register.
- Instruction FLDCW is used to load the value into the control register.

Control Register



- IC Infinity control
- RC Rounding control
- PC Precision control
- PM Precision control
- UM Underflow mask
- OM Overflow mask
- ZM Division by zero mask
- DM Denormalized operand mask
- IM Invalid operand mask

Control Register (cont..)

- IC –Infinity control selects either affine or projective infinity. Affine allows positive and negative infinity, while projective assumes infinity

  is unsigned.
- RC –Rounding control determines the type of rounding.

INFINITY CONTROL
0 = Projective
1 = Affine

ROUNDING CONTROL
00=Round to nearest or even
01=Round down towards minus infinity
10=Round up towards plus infinity
11=Chop or truncate towards zero

Control Register

- PC- Precision control sets the precision of he result as define in table
- Exception Masks – It Determines whether the error indicated by the exception affects the error bit in the status register. If a logic1 is placed in one of the exception control bits, corresponding status register bit is masked off.

PRECISION CONTROL

00=Single precision (short)

01=Reserved

10=Double precision (long)

11=Extended precision (temporary)

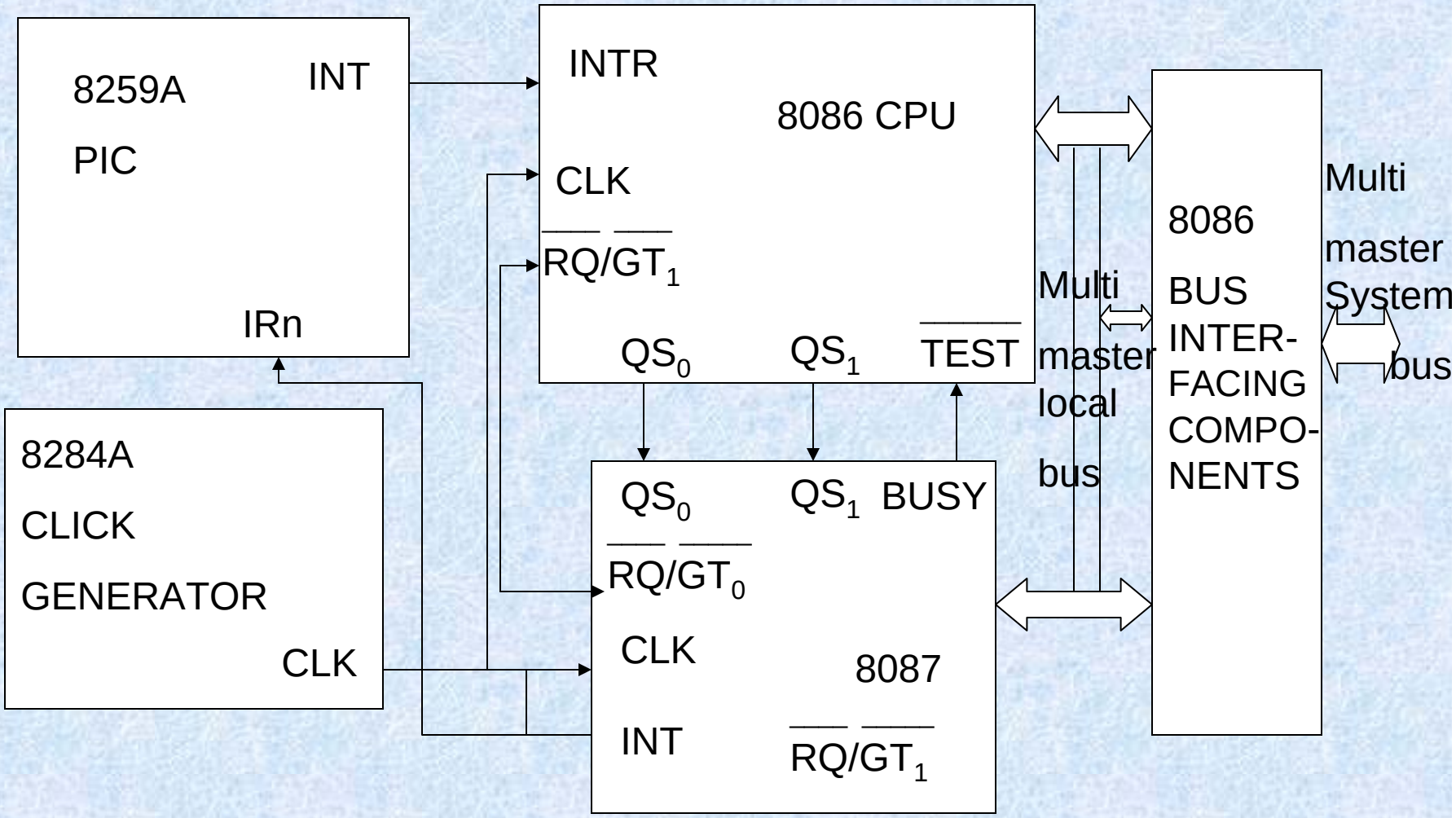
Numeric Execution Unit

- This performs all operations that access and manipulate the numeric data in the coprocessor's registers.
- Numeric registers in NUE are 80 bits wide.
- NUE is able to perform arithmetic, logical and transcendental operations as well as supply a small number of mathematical constants from its on-chip ROM.
- Numeric data is routed into two parts ways

  a 64 bit mantissa bus and

  a 16 bit sign/exponent bus.

Circuit Connection for 8086 – 8087 (cont.)



Circuit Connection for 8086 – 8087 (cont.)

- Multiplexed address-data bus lines are connected directly from the 8086 to 8087.
- The status lines and the queue status lines connected directly from 8086 to 8087.
- The Request/Grant signal $\overline{RQ}/\overline{GT}_0$ of 8087 is connected to $\overline{RQ}/\overline{GT}_1$ of 8086.
- BUSY signal 8087 is connected to TEST pin of 8086.
- Interrupt output INT of the 8087 to NMI input of 8086. This intimates an error condition.

Circuit Connection for 8086 – 8087 (cont.)

- The main purpose of the circuitry between the INT output of 8087 and the NMI input is to make sure that an NMI signal is not present upon reset, to make it possible to mask NMI input and to make it possible for other devices to cause an NMI interrupt.
- BHE pin is connected to the system BHE line to enable the upper bank of memory.
- The RQ/GT_1 input is available so that another coprocessor such as 8089 I/O processor can be connected and function in parallel with the 8087.

Circuit Connection for 8086 – 8087 (cont.)

- One type of Cooperation between the two processors that you need to know about it is how the 8087 transfers data between memory and its internal registers.
- When 8086 reads an 8087 instruction that needs data from memory or wants to send data to memory, the 8086 sends out the memory address code in the instruction and sends out the appropriate memory read or memory write signal to transfer a word of data.

Circuit Connection for 8086 – 8087 (cont.)

- In the case of memory read, the addressed word will be kept on the data bus by the memory. The 8087 then simply reads the word of data bus. The 8086 ignores this word .If the 8087 only needs this one word of data, it can then go on and executes its instruction.
- Some 8087 instructions need to read in or write out up to 80-bit word. For these cases 8086 outputs the address of the first data word on the address bus and outputs the appropriate control signal.

Circuit Connection for 8086 – 8087 (cont.)

- The 8087 reads the data word on the data bus by memory or writes a data word to memory on the data bus. The 8087 grabs the 20-bit physical address that was output by the 8086.To transfer additional words it needs to/from memory, the 8087 then takes over the buses from 8086.
- To take over the bus, the 8087 sends out a low-going pulse on $\overline{RQ}/\overline{GT_0}$ pin. The 8086 responds to this by sending another low going pulse back to the $\overline{RQ}/\overline{GT_0}$ pin of 8087 and by floating its buses.

Circuit Connection for 8086 – 8087 (cont.)

- The 8087 then increments the address it grabbed during the first transfer and outputs the incremented address on the address bus. When the 8087 output a memory read or memory write signal, another data word will be transferred to or from the 8087.
- The 8087 continues the process until it has transferred all the data words required by the instruction to/from memory.

Circuit Connection for 8086 – 8087 (cont.)

- When the 8087 is using the buses for its data transfer, it sends another low-going pulse out on its $\overline{RQ}/\overline{GT_0}$ pin to 8086 to know it can have the buses back again.

The next type of the synchronization between the host processor and the coprocessor is that required to make sure the 8086 hast does not attempt to execute the next instruction before the 8087 has completed an instruction.

Circuit Connection for 8086 – 8087 (cont.)

- Taking one situation, in the case where the 8086 needs the data produced by the execution of an 8087 instruction to carry out its next instruction.
- In the instruction sequence for example the 8087 must complete the ***FSTSW STATUS*** instruction before the 8086 will have the data it needs to execute the ***MOV AX , STATUS*** instruction.
- Without some mechanism to make the 8086 wait until the 8087 completes the FSTSW instruction, the 8086 will go on and execute the ***MOV AX , STATUS*** with erroneous data .
- We solve this problem by connecting the 8087 BUSY output to the TEST pin of the 8086 and putting on the WAIT instruction in the program.

Circuit Connection for 8086 – 8087 (cont.)

- While 8087 is executing an instruction it asserts its BUSY pin high. When it is finished with an instruction, the 8087 will drop its BUSY pin low. Since the BUSY pin from 8087 is connected to the TEST pin 8086 the processor can check its pin of 8087 whether it finished it instruction or not.
- You place the 8086 WAIT instruction in your program after the 8087 FSTSW instruction .When 8086 executes the WAIT instruction it enters an internal loop where it repeatedly checks the logic level on the TEST input. The 8086 will stay in this loop until it finds the TEST input asserted low, indicating the 8087 has completed its instruction. The 8086 will then exit the internal loop, fetch and execute the next instruction.

Example (cont..)

```
FSTSW       STATUS      ;copy  8087 status word to memory
MOV         AX, STATUS  ;copy status word to AX to check
                        ; bits
```

(a)

- In this set of instructions we are not using WAIT instruction. Due to this the flow of execution of command will takes place continuously even though the previous instruction had not finished it's completion of its work .so we may lost data .

Example (cont..)

```
FSTSW       STATUS      ;copy 8087 status word to memory
FWAIT                   ;wait for 8087 to finish before-
                        ; doing next 8086 instruction
MOV         AX,STATUS   ;copy status word to AX to check
                        ; bits
```

(b)

- In this code we are adding up of FWAIT instruction so that it will stop the execution of the command until the above instruction is finishes it's work .so that you are not loosing data and after that you will allow to continue the execution of instructions.

Circuit Connection for 8086 – 8087 (cont.)

- Another case where you need synchronization of the processor and the coprocessor is the case where a program has several 8087 instructions in sequence.
- The 8087 are executed only one instruction at a time so you have to make sure that 8087 has completed one instruction before you allow the 8086 to fetch the next 8087 instruction from memory.
- Here again you use the BUSY-$\overline{\text{TEST}}$ connection and the FWAIT instruction to solve the problem. If you are hand coding, you can just put the 8086 WAIT(FWAIT) instruction after each instruction to make sure that instruction is completed before going on to next.

Circuit Connection for 8086 – 8087

- If you are using the assembler which accepts 8087 mnemonics, the assembler will automatically insert the 8-bit code for the WAIT instruction ,10011011 binary (9BH), as the first byte of the code for 8087 instruction.

Interfacing (cont..)

- Multiplexed address-data bus lines are connected directly from the 8086 to 8087.
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- The Request/Grant signal RQ/GT0 of 8087 is connected to RQ/GT1 of 8086.
- BUSY signal 8087 is connected to TEST pin of 8086.
- Interrupt output INT of the 8087 to NMI input of 8086. This intimates an error condition.
- A WAIT instruction is passed to keep looking at its TEST pin, until it finds pin Low to indicates that the 8087 has completed the computation.

Interfacing

- SYNCHRONIZATION must be established between the processor and coprocessor in two situations.

  a) The execution of an ESC instruction that require the participation of the NUE must not be initiated if the NUE has not completed the execution of the previous instruction.

  b) When a processor instruction accesses a memory location that is an operand of a previous coprocessor instruction .In this case CPU must synchronize with NPX to ensure that it has completed its instruction.

  Processor WAIT instruction is provided.