8259A

- If we are working with an 8086, we have a problem here because the 8086 has only two interrupt inputs, NMI and INTR.

- If we save NMI for a power failure interrupt, this leaves only one interrupt for all the other applications. For applications where we have interrupts from multiple source, we use an external device called a *priority interrupt controller* (PIC) to the interrupt signals into a single interrupt input on the processor.

Architecture and Signal Descriptions of 8259A (cont..)

- The architectural block diagram of 8259A is shown in fig1. The functional explication of each block is given in the following text in brief.

- **Interrupt Request Register (RR)**: The interrupts at IRQ input lines are handled by Interrupt Request internally. IRR stores all the interrupt request in it in order to serve them one by one on the priority basis.

- **In-Service Register (ISR)**: This stores all the interrupt requests those are being served, i.e. ISR keeps a track of the requests being served.
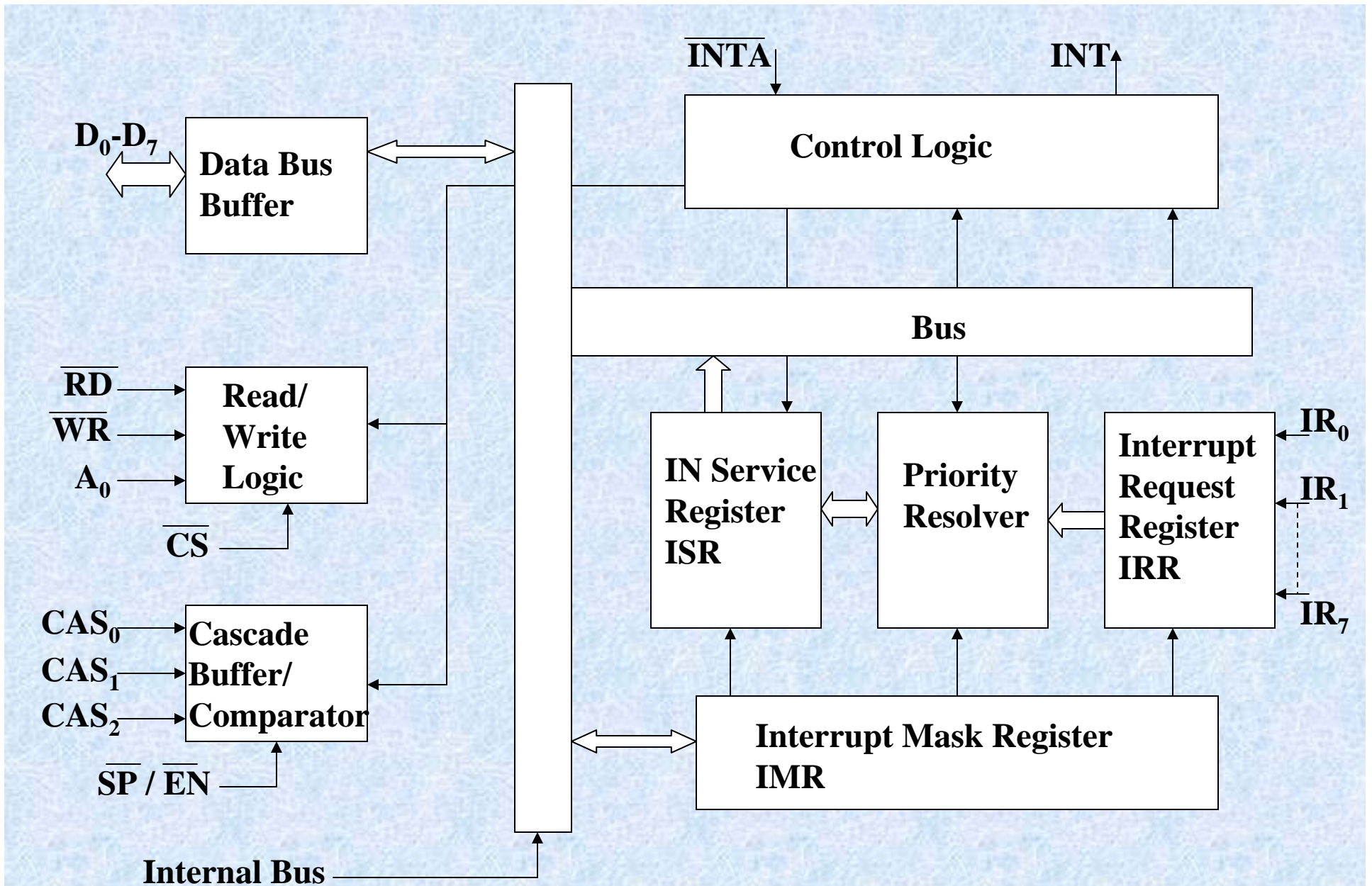
Fig:1   8259A Block Diagram

Architecture and Signal Descriptions of 8259A (cont..)

- **Priority Resolver :** This unit determines the priorities of the interrupt requests appearing simultaneously. The highest priority is selected and stored into the corresponding bit of ISR during $\overline{INTA}$ pulse. The IR_0 has the highest priority while the IR_7 has the lowest one, normally in fixed priority mode. The priorities however may be altered by programming the 8259A in rotating priority mode.

- **Interrupt Mask Register (IMR)** : This register stores the bits required to mask the interrupt inputs. IMR operates on IRR at the direction of the Priority Resolver.

Architecture and Signal Descriptions of 8259A (cont..)

- **Interrupt Control Logic**: This block manages the interrupt and interrupt acknowledge signals to be sent to the CPU for serving one of the eight interrupt requests. This also accepts the interrupt acknowledge (INTA) signal from CPU that causes the 8259A to release vector address on to the data bus.

- **Data Bus Buffer** : This tristate bidirectional buffer interfaces internal 8259A bus to the microprocessor system data bus. Control words, status and vector information pass through data buffer during read or write operations.

Architecture and Signal Descriptions of 8259A (cont..)

- **Read/Write Control Logic**: This circuit accepts and decodes commands from the CPU. This block also allows the status of the 8259A to be transferred on to the data bus.

- **Cascade Buffer/Comparator**: This block stores and compares the ID's all the 8259A used in system. The three I/O pins CASO-2 are outputs when the 8259A is used as a master. The same pins act as inputs when the 8259A is in slave mode. The 8259A in master mode sends the ID of the interrupting slave device on these lines. The slave thus selected, will send its preprogrammed vector address on the data bus during the next $\overline{INTA}$ pulse.
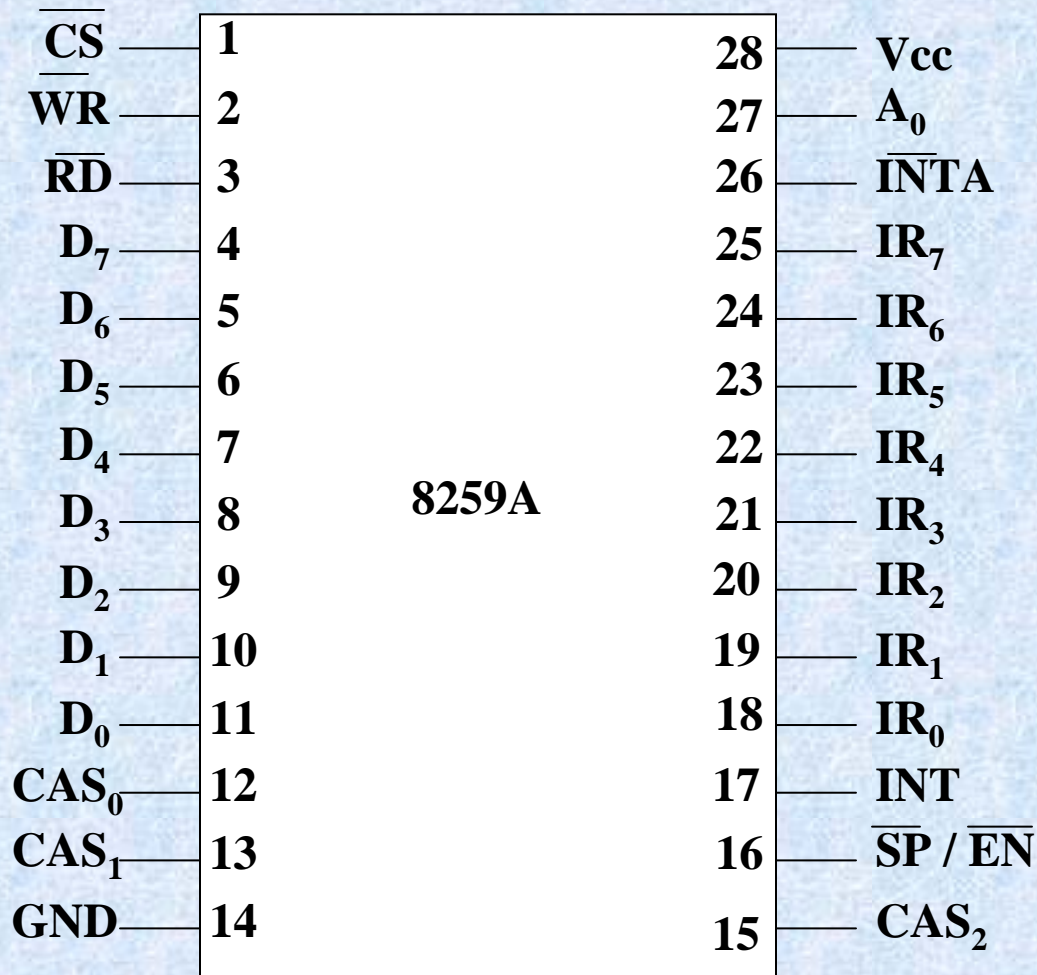
			8259A			
$\overline{CS}$	—	1		28	—	Vcc
$\overline{WR}$	—	2		27	—	A_0
$\overline{RD}$	—	3		26	—	$\overline{INTA}$
D_7	—	4		25	—	IR_7
D_6	—	5		24	—	IR_6
D_5	—	6		23	—	IR_5
D_4	—	7		22	—	IR_4
D_3	—	8		21	—	IR_3
D_2	—	9		20	—	IR_2
D_1	—	10		19	—	IR_1
D_0	—	11		18	—	IR_0
CAS_0	—	12		17	—	INT
CAS_1	—	13		16	—	$\overline{SP} / \overline{EN}$
GND	—	14		15	—	CAS_2

Fig : 8259 Pin Diagram

Architecture and Signal Descriptions of 8259A (cont..)

- $\overline{\text{CS}}$: This is an active-low chip select signal for enabling $\overline{\text{RD}}$ and $\overline{\text{WR}}$ operations of 8259A. $\overline{\text{INTA}}$ function is independent of $\overline{\text{CS}}$.

- $\overline{\text{WR}}$: This pin is an active-low write enable input to 8259A. This enables it to accept command words from CPU.

- $\overline{\text{RD}}$: This is an active-low read enable input to 8259A. A low on this line enables 8259A to release status onto the data bus of CPU.

- D_0-D_7 : These pins from a bidirectional data bus that carries 8-bit data either to control word or from status word registers. This also carries interrupt vector information.

Architecture and Signal Descriptions of 8259A (cont..)

- **CAS_0 – CAS_2 Cascade Lines** : A signal 8259A provides eight vectored interrupts. If more interrupts are required, the 8259A is used in cascade mode. In cascade mode, a master 8259A along with eight slaves 8259A can provide upto 64 vectored interrupt lines. These three lines act as select lines for addressing the slave 8259A.

- **$\overline{PS}/\overline{EN}$** : This pin is a dual purpose pin. When the chip is used in buffered mode, it can be used as buffered enable to control buffer transreceivers. If this is not used in buffered mode then the pin is used as input to designate whether the chip is used as a master ($\overline{SP}$ =1) or slave ($\overline{EN}$ = 0).

Architecture and Signal Descriptions of 8259A (cont..)

- **INT** : This pin goes high whenever a valid interrupt request is asserted. This is used to interrupt the CPU and is connected to the interrupt input of CPU.

- **IR$_0$ – IR$_7$ (Interrupt requests)** :These pins act as inputs to accept interrupt request to the CPU. In edge triggered mode, an interrupt service is requested by raising an IR pin from a low to a high state and holding it high until it is acknowledged, and just by latching it to high level, if used in level triggered mode.

Architecture and Signal Descriptions of 8259A (cont..)

- **$\overline{\text{INTA}}$ (Interrupt acknowledge)**: This pin is an input used to strobe-in 8259A interrupt vector data on to the data bus. In conjunction with $\overline{\text{CS}}$, $\overline{\text{WR}}$ and $\overline{\text{RD}}$ pins, this selects the different operations like, writing command words, reading status word, etc.

- The device 8259A can be interfaced with any CPU using either polling or interrupt. In polling, the CPU keeps on checking each peripheral device in sequence to ascertain if it requires any service from the CPU. If any such service request is noticed, the CPU serves the request and then goes on to the next device in sequence.

Architecture and Signal Descriptions of 8259A (cont..)

- After all the peripheral device are scanned as above the CPU again starts from first device.

- This type of system operation results in the reduction of processing speed because most of the CPU time is consumed in polling the peripheral devices.

- In the interrupt driven method, the CPU performs the main processing task till it is interrupted by a service requesting peripheral device.

- The net processing speed of these type of systems is high because the CPU serves the peripheral only if it receives the interrupt request.

Architecture and Signal Descriptions of 8259A.

- If more than one interrupt requests are received at a time, all the requesting peripherals are served one by one on priority basis.

- This method of interfacing may require additional hardware if number of peripherals to be interfaced is more than the interrupt pins available with the CPU.

Interrupt Sequence in an 8086 system (cont..)

- The Interrupt sequence in an 8086-8259A system is described as follows:

1. One or more IR lines are raised high that set corresponding IRR bits.

2. 8259A resolves priority and sends an INT signal to CPU.

3. The CPU acknowledge with INTA pulse.

4. Upon receiving an INTA signal from the CPU, the highest priority ISR bit is set and the corresponding IRR bit is reset. The 8259A does not drive data during this period.

Interrupt Sequence in an 8086 system.

5. The 8086 will initiate a second INTA pulse. During this period 8259A releases an 8-bit pointer on to a data bus from where it is read by the CPU.

6. This completes the interrupt cycle. The ISR bit is reset at the end of the second INTA pulse if automatic end of interrupt (AEOI) mode is programmed. Otherwise ISR bit remains set until an appropriate EOI command is issued at the end of interrupt subroutine.

Command Words of 8259A (cont..)

- The command words of 8259A are classified in two groups

1. Initialization command words (ICW) and

2. Operation command words (OCW).

- Initialization Command Words (ICW): Before it starts functioning, the 8259A must be initialized by writing two to four command words into the respective command word registers. These are called as initialized command words.

Command Words of 8259A (cont..)

- If $A_0 = 0$ and $D_4 = 1$, the control word is recognized as ICW_1. It contains the control bits for edge/level triggered mode, single/cascade mode, call address interval and whether ICW_4 is required or not.

- If $A_0 = 1$, the control word is recognized as ICW_2. The ICW_2 stores details regarding interrupt vector addresses. The initialisation sequence of 8259A is described in form of a flow chart in fig 3 below.

- The bit functions of the ICW_1 and ICW_2 are self explanatory as shown in fig below.
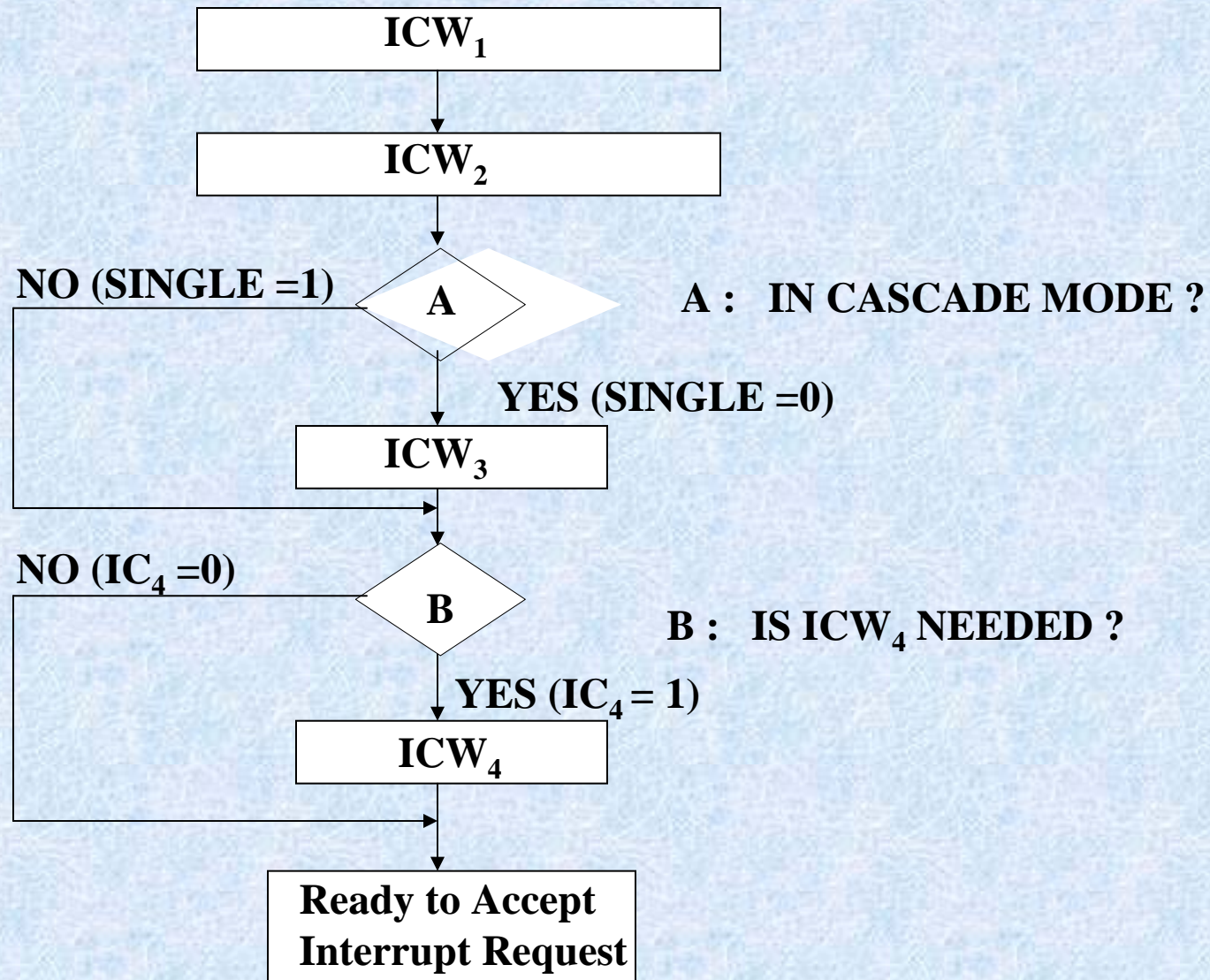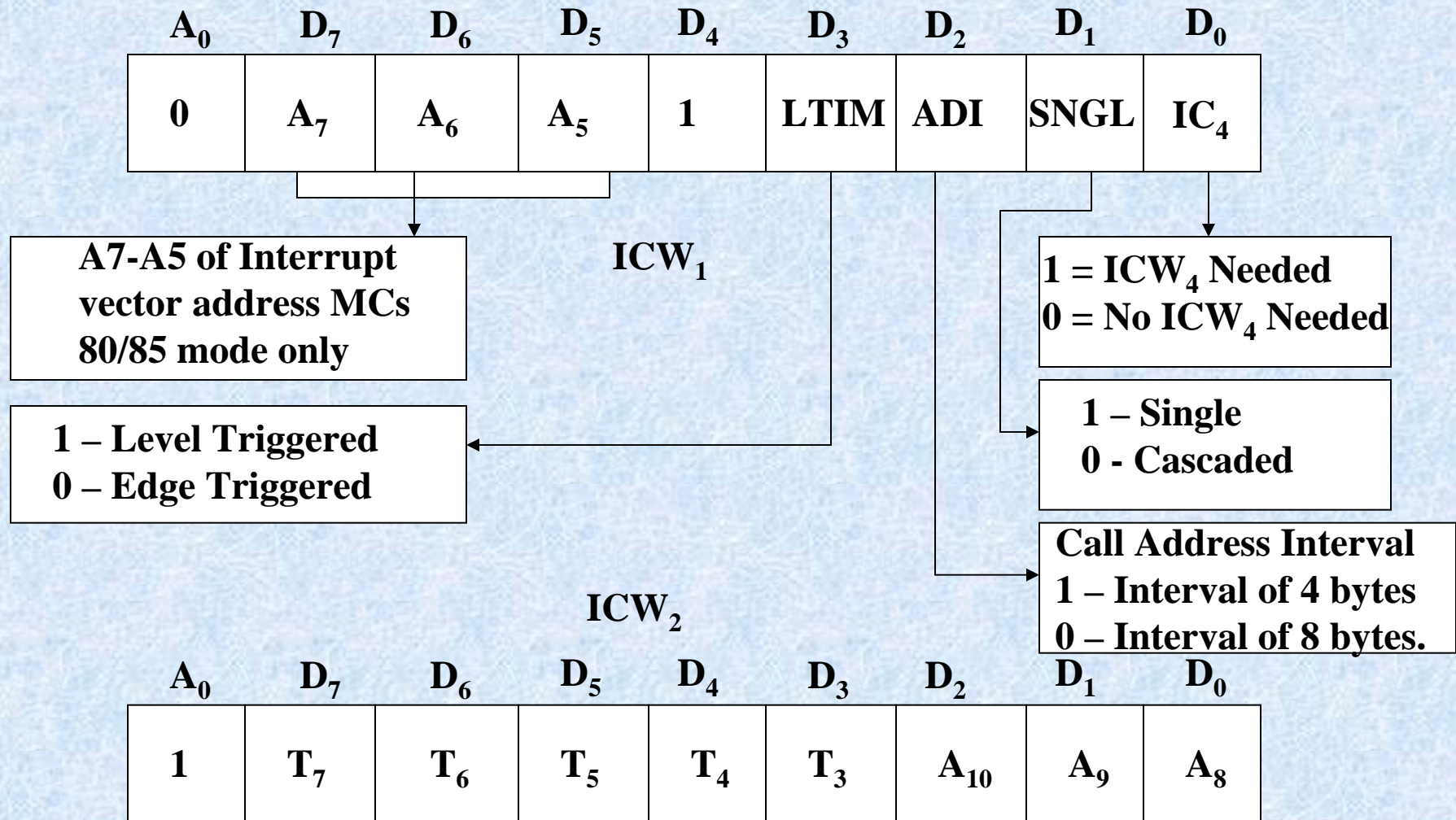
Fig 3: Initialisation Sequence of 8259A

The flowchart shows:

- ICW_1
- ICW_2
- A : IN CASCADE MODE ?
  - NO (SINGLE =1)
  - YES (SINGLE =0)
- ICW_3
- B : IS ICW_4 NEEDED ?
  - NO (IC_4 =0)
  - YES (IC_4 = 1)
- ICW_4
- Ready to Accept Interrupt Request

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
0	A_7	A_6	A_5	1	LTIM	ADI	SNGL	IC_4

A7-A5 of Interrupt vector address MCs 80/85 mode only

ICW_1

1 = ICW_4 Needed
0 = No ICW_4 Needed

1 – Level Triggered
0 – Edge Triggered

1 – Single
0 - Cascaded

Call Address Interval
1 – Interval of 4 bytes
0 – Interval of 8 bytes.

ICW_2

A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
1	T_7	T_6	T_5	T_4	T_3	A_{10}	A_9	A_8

- T_7 – T3 are A3 – A0 of interrupt address
- A_{10} – A_9, A_8 – Selected according to interrupt request level.
     They are not the address lines of Microprocessor
- A0 =1 selects ICW_2

Fig 4 : Instruction Command Words ICW_1 and ICW_2

Command Words of 8259A (cont..)

- Once ICW_1 is loaded, the following initialization procedure is carried out internally.

a. The edge sense circuit is reset, i.e. by default 8259A interrupts are edge sensitive.

b. IMR is cleared.

c. IR7 input is assigned the lowest priority.

d. Slave mode address is set to 7.

e. Special mask mode is cleared and status read is set to IRR.

f. If $IC_4 = 0$, all the functions of ICW_4 are set to zero. Master/Slave bit in ICW_4 is used in the buffered mode only.

Command Words of 8259A (cont..)

- In an 8085 based system A_{15}-A_8 of the interrupt vector address are the respective bits of ICW_2.

- In 8086 based system A_{15}-A_{11} of the interrupt vector address are inserted in place of $T_7 - T_3$ respectively and the remaining three bits A_8, A_9, A_{10} are selected depending upon the interrupt level, i.e. from 000 to 111 for IR_0 to IR_7.

- ICW_1 and ICW_2 are compulsory command words in initialization sequence of 8259A as is evident from fig, while ICW_3 and ICW_4 are optional. The ICW_3 is read only when there are more than one 8259A in the system, cascading is used (SNGL=0).

Command Words of 8259A (cont..)

- The SNGL bit in ICW_1 indicates whether the 8259A in the cascade mode or not. The ICW_3 loads an 8-bit slave register. It detailed functions are as follows.

- In master mode [$\overline{SP} = 1$ or in buffer mode M/S = 1 in ICW_4], the 8-bit slave register will be set bit-wise to 1 for each slave in the system as in fig 5.

- The requesting slave will then release the second byte of a CALL sequence. In slave mode [SP=0 or if BUF =1 and M/S = 0 in ICW_4] bits D_2 to D_0 identify the slave, i.e. 000 to 111 for slave 1 to slave 8. The slave compares the cascade inputs with these bits and if they are equal, the second byte of the CALL sequence is released by it on the data bus.

Master mode ICW$_3$

A$_0$	D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
1	S$_7$	S$_6$	S$_5$	S$_4$	S$_3$	S$_2$	S$_1$	S$_0$

Sn = 1-IRn Input has a slave
= 0 – IRn Input does not have a slave

Slave mode ICW$_3$

A$_0$	D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
1	0	0	0	0	0	ID$_2$	ID$_1$	ID$_0$

D$_2$D$_1$D$_0$ – 000 to 111 for IR$_0$ to IR$_7$ or slave 1 to slave 8

ICW$_4$

A$_0$	D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
1	0	0	0	SFNM	BUF	M/S	AEOI	μPM

Fig : ICW$_3$ in Master and Slave Mode, ICW$_4$ Bit Functions

Command Words of 8259A (cont..)

- **ICW$_4$**: The use of this command word depends on the IC$_4$ bit of ICW$_1$. If IC$_4$=1, IC$_4$ is used, otherwise it is neglected. The bit functions of ICW4 are described as follow:

- **SFNM**: If BUF = 1, the buffered mode is selected. In the buffered mode, SP/EN acts as enable output and the master/slave is determined using the M/S bit of ICW$_4$.

- **M/S**: If M/S = 1, 8259A is a master. If M/S =0, 8259A is slave. If BUF = 0, M/S is to be neglected.

- **AEOI**: If AEOI = 1, the automatic end of interrupt mode is selected.

Command Words of 8259A (cont..)

- **µPM** : If the µPM bit is 0, the Mcs-85 system operation is selected and if µPM=1, 8086/88 operation is selected.

- **Operation Command Words:** Once 8259A is initialized using the previously discussed command words for initialisation, it is ready for its normal function, i.e. for accepting the interrupts but 8259A has its own way of handling the received interrupts called as modes of operation. These modes of operations can be selected by programming, i.e. writing three internal registers called as operation command words.

Command Words of 8259A (cont..)

- In the three operation command words OCW_1, OCW_2 and OCW_3 every bit corresponds to some operational feature of the mode selected, except for a few bits those are either 1 or 0. The three operation command words are shown in fig with the bit selection details.

- OCW_1 is used to mask the masked and if it is 0 the request is enabled. In OCW_2 the three bits, R, SL and EOI control the end of interrupt, the rotate mode and their combinations as shown in fig below.

- The three bits L_2, L_1 and L_0 in OCW_2 determine the interrupt level to be selected for operation, if SL bit is active i.e. 1.

Command Words of 8259A (cont..)

- The details of OCW_2 are shown in fig.

- In operation command word 3 (OCW_3), if the ESMM bit, i.e. enable special mask mode bit is set to 1, the SMM bit is neglected. If the SMM bit, i.e. special mask mode. When ESMM bit is 0 the SMM bit is neglected. If the SMM bit. i.e. special mask mode bit is 1, the 8259A will enter special mask mode provided ESMM=1.

- If ESMM=1 and SMM=0, the 8259A will return to the normal mask mode. The details of bits of OCW_3 are given in fig along with their bit definitions.
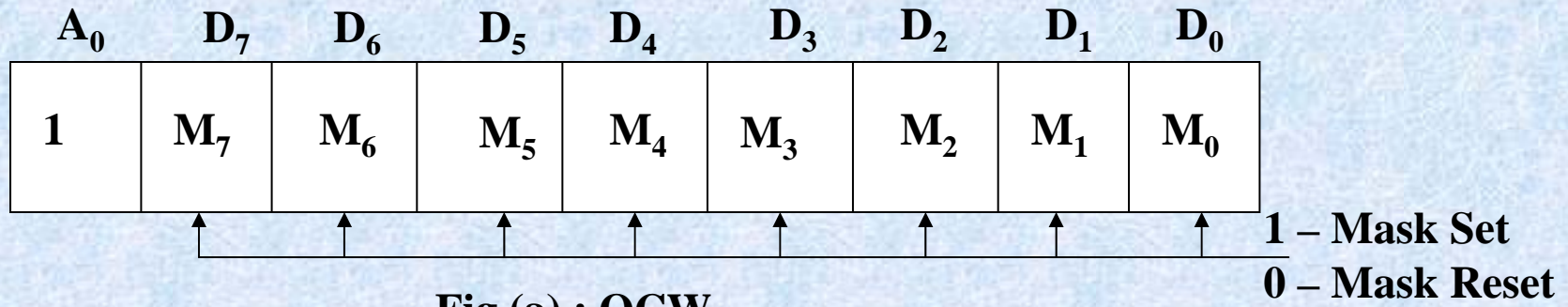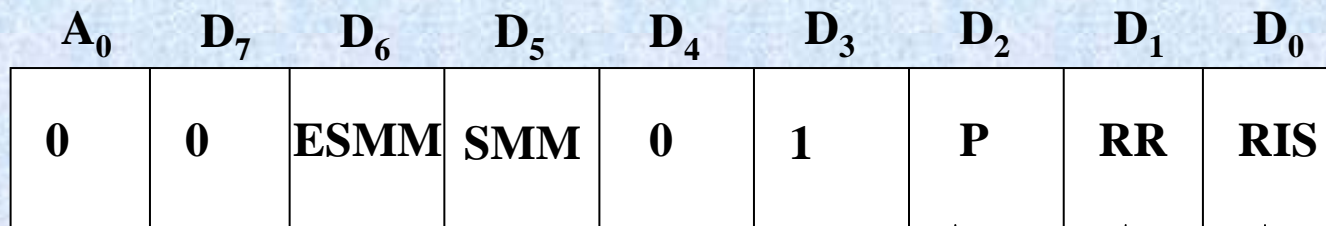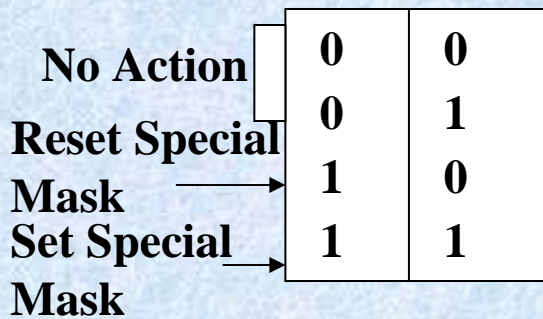
Fig (a) : OCW$_1$

Fig (b) : OCW$_3$
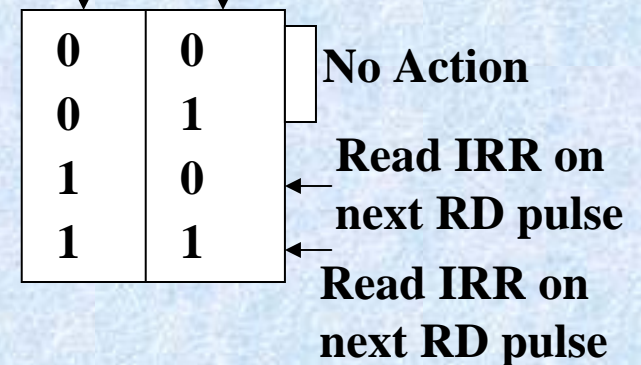
Fig : Operation Command Words

Fig (c) :OCW$_2$

A$_0$	D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
1	R	SL	EOI	0	0	L$_2$	L$_1$	L$_0$

0	1	2	3	4	5	6	7
0	1	0	0	0	1	0	1
0	0	1	1	0	0	1	1
0	0	0	0	1	1	1	1

END OF INTERRUPT

0	0	1	NON-SPECIFIC EOI COMMAND
0	1	1	SPECIFIC EOI COMMAND
1	0	1	ROTATE ON NON-SPECIFIC EOI MODE (SET)
1	0	0	ROTATE IN AUTOMATIC EOI MODE (SET)
0	0	0	ROTATE IN AUTOMATIC EOI (CLEAR)
1	1	1	ROTATE ON SPECIFIC EOI COMMAND
1	1	0	SET PRIORITY COMMAND*
0	1	0	NO OPERATION

AUTOMATIC ROTATION

SPECIFIC ROTATION
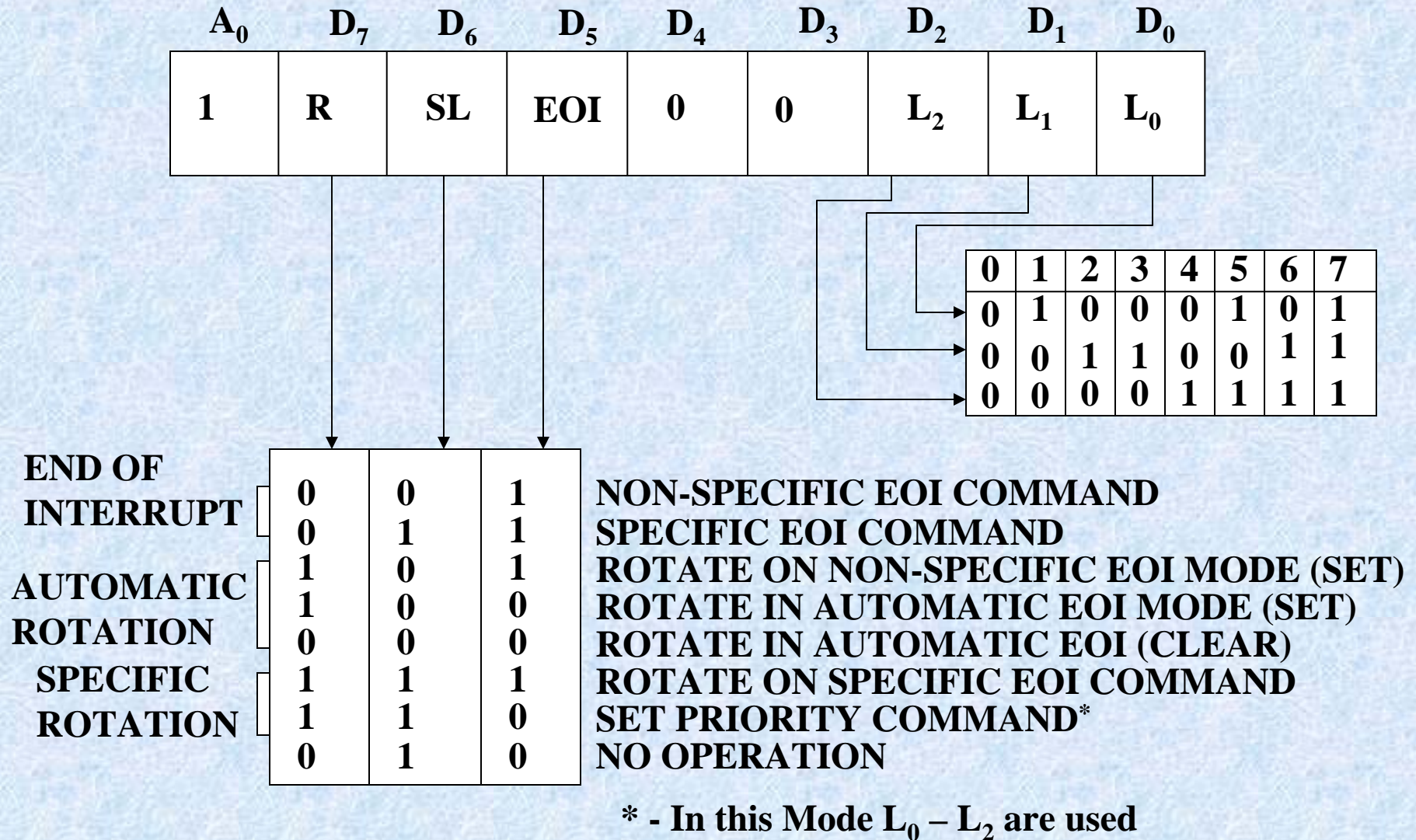
* - In this Mode L$_0$ – L$_2$ are used

Fig : Operation Command Word

Operating Modes of 8259 (cont..)

- The different modes of operation of 8259A can be programmed by setting or resting the appropriate bits of the ICW or OCW as discussed previously. The different modes of operation of 8259A are explained in the following.

- **Fully Nested Mode** : This is the default mode of operation of 8259A. IR0 has the highest priority and IR$_7$ has the lowest one. When interrupt request are noticed, the highest priority request amongst them is determined and the vector is placed on the data bus. The corresponding bit of ISR is set and remains set till the microprocessor issues an EOI command just before returning from the service routine or the AEOI bit is set.

Operating Modes of 8259 (cont..)

- If the ISR (in service) bit is set, all the same or lower priority interrupts are inhibited but higher levels will generate an interrupt, that will be acknowledge only if the microprocessor interrupt enable flag IF is set. The priorities can afterwards be changed by programming the rotating priority modes.

- **End of Interrupt (EOI)** : The ISR bit can be reset either with AEOI bit of ICW1 or by EOI command, issued before returning from the interrupt service routine. There are two types of EOI commands specific and non-specific. When 8259A is operated in the modes that preserve fully nested structure, it can determine which ISR bit is to be reset on EOI.

Operating Modes of 8259 (cont..)

- When non-specific EOI command is issued to 8259A it will be automatically reset the highest ISR bit out of those already set.

- When a mode that may disturb the fully nested structure is used, the 8259A is no longer able to determine the last level acknowledged. In this case a specific EOI command is issued to reset a particular ISR bit. An ISR bit that is masked by the corresponding IMR bit, will not be cleared by non-specific EOI of 8259A, if it is in special mask mode.

- **Automatic Rotation** : This is used in the applications where all the interrupting devices are of equal priority.

Operating Modes of 8259 (cont..)

- In this mode, an interrupt request IR level receives priority after it is served while the next device to be served gets the highest priority in sequence. Once all the device are served like this, the first device again receives highest priority.

- **Automatic EOI Mode** : Till AEOI=1 in ICW_4, the 8259A operates in AEOI mode. In this mode, the 8259A performs a non-specific EOI operation at the trailing edge of the last INTA pulse automatically. This mode should be used only when a nested multilevel interrupt structure is not required with a single 8259A.

Operating Modes of 8259 (cont..)

- **Specific Rotation** : In this mode a bottom priority level can be selected, using L2, L1 and L0 in OCW_2 and R=1, SL=1, EOI=0.

- The selected bottom priority fixes other priorities. If IR_5 is selected as a bottom priority, then IR_5 will have least priority and IR4 will have a next higher priority. Thus IR_6 will have the highest priority.

- These priorities can be changed during an EOI command by programming the rotate on specific EOI command in OCW_2.

Operating Modes of 8259 (cont..)

- **Specific Mask Mode**: In specific mask mode, when a mask bit is set in OCW_1, it inhibits further interrupts at that level and enables interrupt from other levels, which are not masked.

- **Edge and Level Triggered Mode** : This mode decides whether the interrupt should be edge triggered or level triggered. If bit LTIM of ICW_1 =0 they are edge triggered, otherwise the interrupts are level triggered.

- **Reading 8259 Status** : The status of the internal registers of 8259A can be read using this mode. The OCW_3 is used to read IRR and ISR while OCW_1 is used to read IMR. Reading is possible only in no polled mode.

Operating Modes of 8259 (cont..)

- **Poll Command** : In polled mode of operation, the INT output of 8259A is neglected, though it functions normally, by not connecting INT output or by masking INT input of the microprocessor. The poll mode is entered by setting P=1 in OCW_3.

- The 8259A is polled by using software execution by microprocessor instead of the requests on INT input. The 8259A treats the next RD pulse to the 8259A as an interrupt acknowledge. An appropriate ISR bit is set, if there is a request. The priority level is read and a data word is placed on to data bus, after RD is activated. A poll command may give more than 64 priority levels.
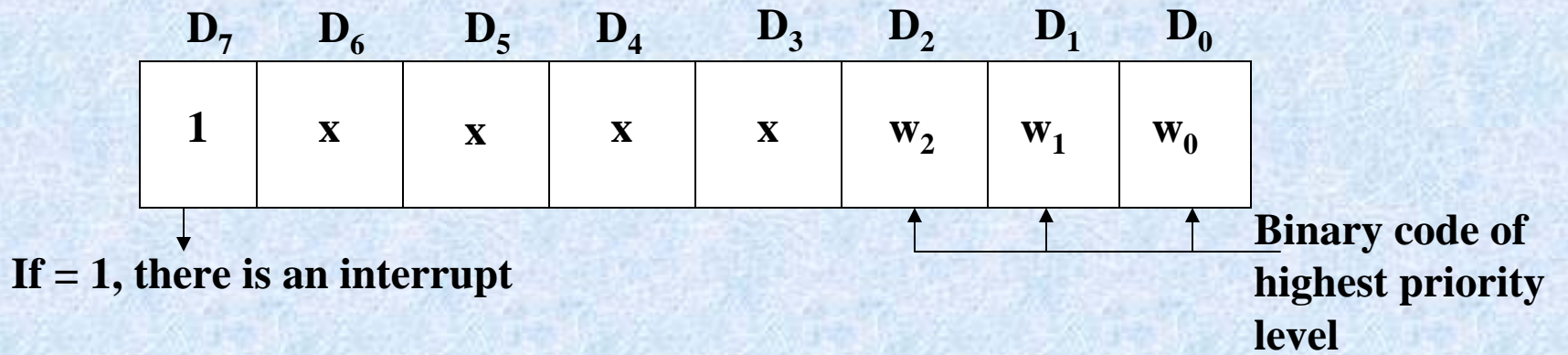
D$_7$	D$_6$	D$_5$	D$_4$	D$_3$	D$_2$	D$_1$	D$_0$
1	x	x	x	x	W$_2$	W$_1$	W$_0$

If = 1, there is an interrupt

Binary code of highest priority level

Fig : Data Word of 8259

Operating Modes of 8259 (cont..)

- **Special Fully Nested Mode** : This mode is used in more complicated system, where cascading is used and the priority has to be programmed in the master using ICW_4. this is somewhat similar to the normal nested mode.

- In this mode, when an interrupt request from a certain slave is in service, this slave can further send request to the master, if the requesting device connected to the slave has higher priority than the one being currently served. In this mode, the master interrupt the CPU only when the interrupting device has a higher or the same priority than the one current being served. In normal mode, other requests than the one being served are masked out.

Operating Modes of 8259 (cont..)

- When entering the interrupt service routine the software has to check whether this is the only request from the slave. This is done by sending a non-specific EOI can be sent to the master, otherwise no EOI should be sent. This mode is important, since in the absence of this mode, the slave would interrupt the master only once and hence the priorities of the slave inputs would have been disturbed.

- **Buffered Mode**: When the 83259A is used in the systems where bus driving buffers are used on data buses. The problem of enabling the buffers exists. The 8259A sends buffer enable signal on $\overline{SP}/\overline{EN}$ pin, whenever data is placed on the bus.

Operating Modes of 8259 (cont..)

- **Cascade Mode** : The 8259A can be connected in a system containing one master and eight slaves (maximum) to handle upto 64 priority levels. The master controls the slaves using CAS_0-CAS_2 which act as chip select inputs (encoded) for slaves.

- In this mode, the slave INT outputs are connected with master IR inputs. When a slave request line is activated and acknowledged, the master will enable the slave to release the vector address during second pulse of $\overline{INTA}$ sequence.

Operating Modes of 8259 (cont..)

- The cascade lines are normally low and contain slave address codes from the trailing edge of the first INTA pulse to the trailing edge of the second INTA pulse. Each 8259A in the system must be separately initialized and programmed to work in different modes. The EOI command must be issued twice, one for master and the other for the slave.

- A separate address decoder is used to activate the chip select line of each 8259A.

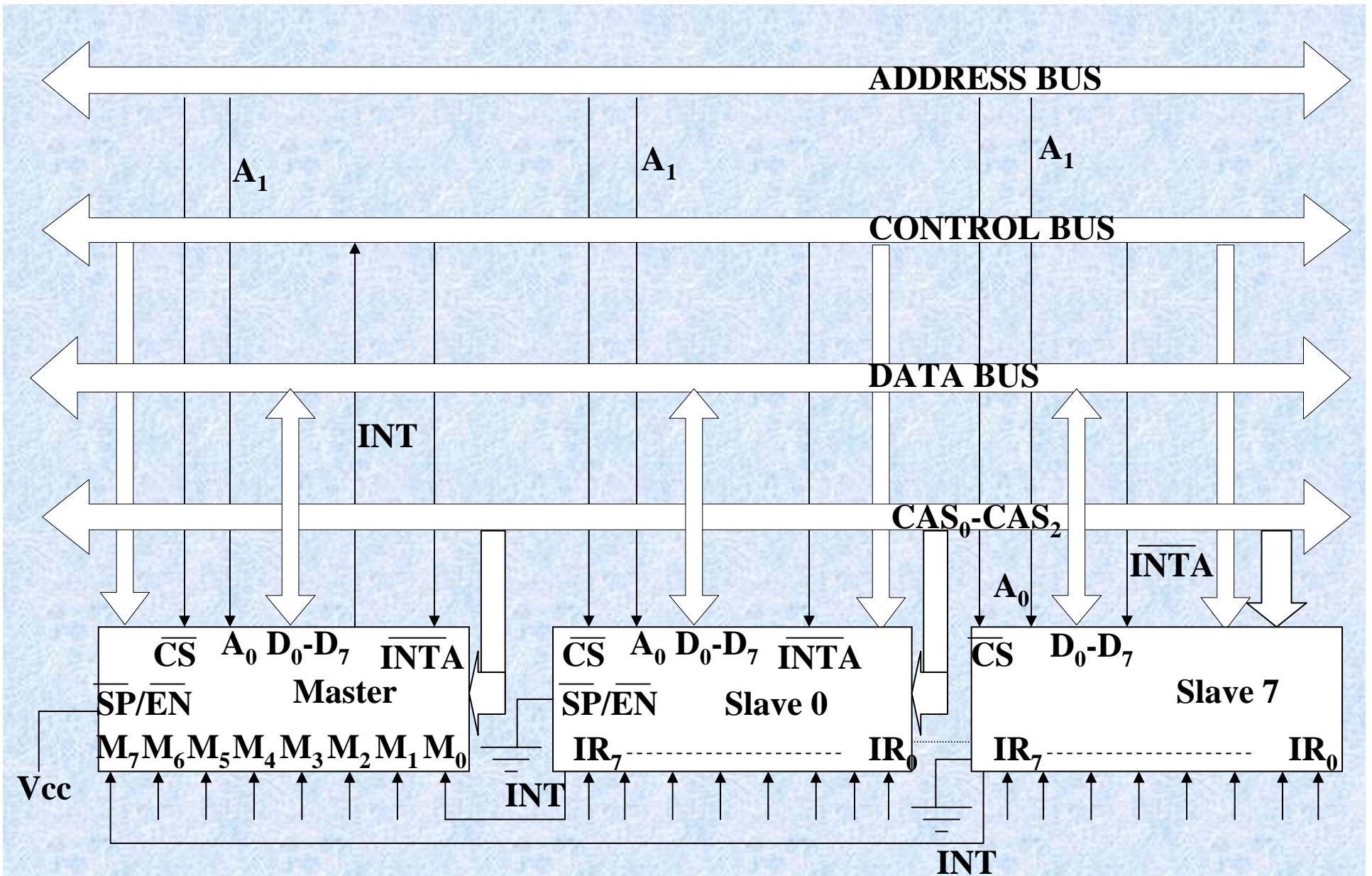- Following Fig shows the details of the circuit connections of 8259A in cascade scheme.

Fig : 8259A in Cascade Mode