

8254

- Compatible with All Intel and Most other Microprocessors
- Handles Inputs from DC to 10 MHz
 - 8 MHz 8254
 - 10 MHz 8254-2
- Status Read-Back Command
- Six Programmable Counter Modes
- Three Independent 16-Bit Counters
- Binary or BCD Counting
- Single a 5V Supply
- Standard Temperature Range

8254 (cont..)

- The Intel 8254 is a counter/timer device designed to solve the common timing control problems in microcomputer system design.
- It provides three independent 16-bit counters, each capable of handling clock inputs up to 10 MHz.
- All modes are software programmable. The 8254 is a superset of the 8253.
- The 8254 uses HMOS technology and comes in a 24-pin plastic or CERDIP package.

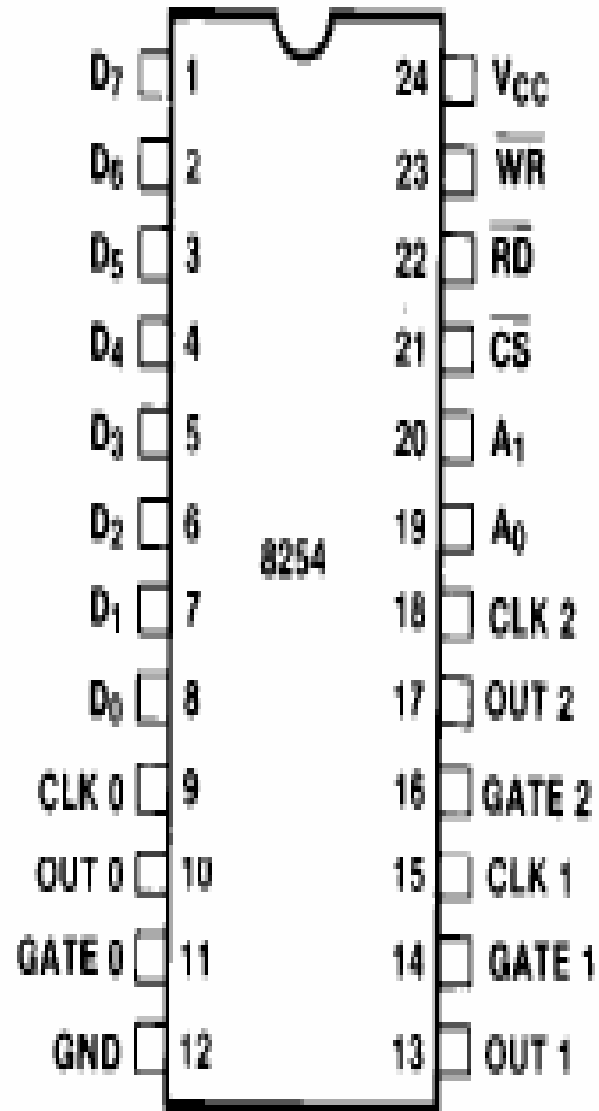


Figure 1. Pin Configuration

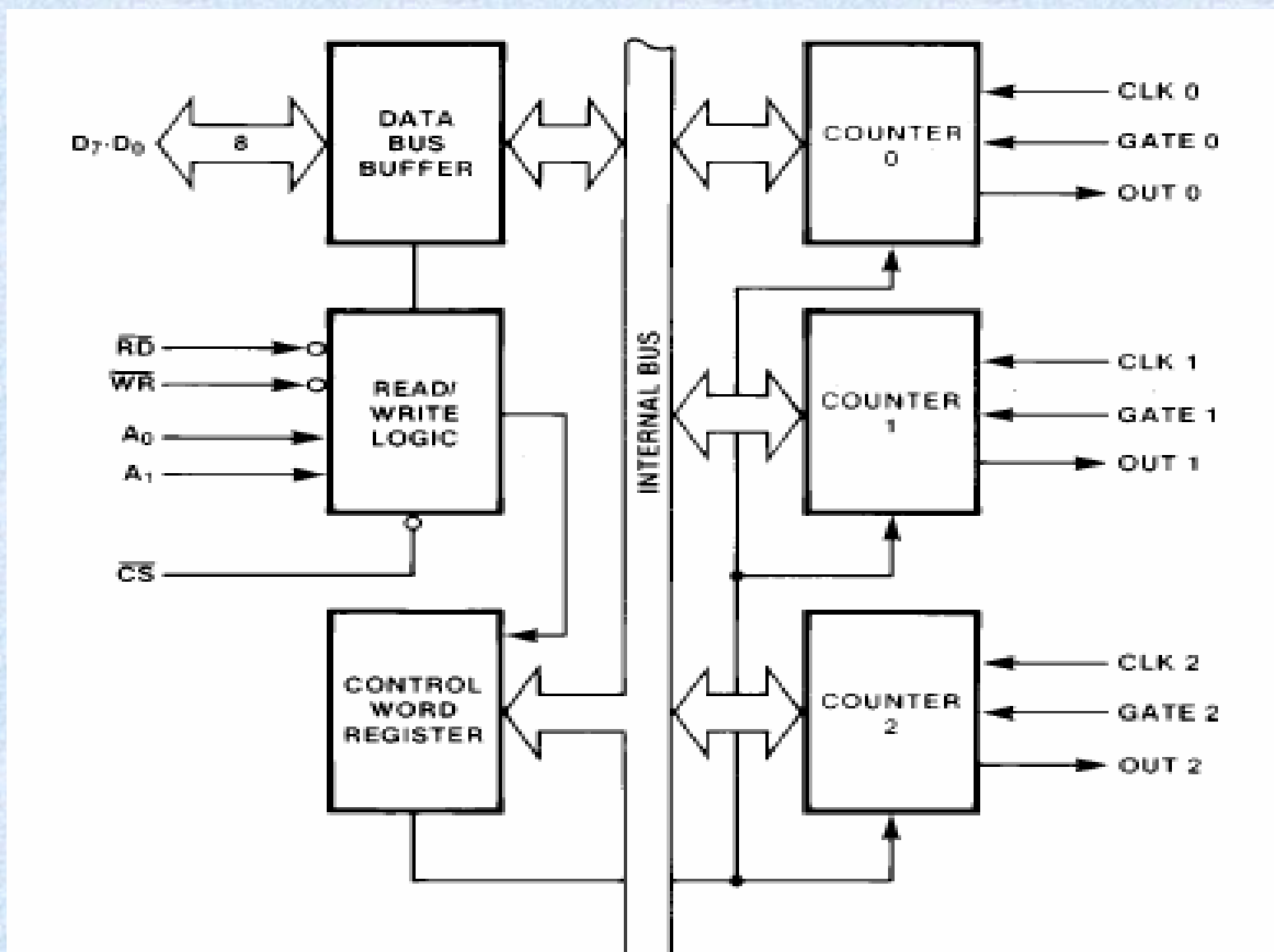


Figure 2. 8254 Block Diagram

Pin Description

Symbol	Pin No.	Type	Name and Function
D7-D0	1 - 8	I/O	DATA: Bi-directional three state data bus lines, connected to system data bus.
CLK 0	9	I	CLOCK 0: Clock input of Counter 0.
OUT 0	10	O	OUTPUT 0: Output of Counter 0.
GATE 0	11	I	GATE 0: Gate input of Counter 0.
GND	12		GROUND: Power supply connection.
VCC	24		POWER: A 5V power supply connection.
$\overline{\text{WR}}$	23	I	WRITE CONTROL: This input is low during CPU write operations.
RD	22	I	READ CONTROL: This input is low during CPU read operations.

Pin Description (cont..)

CS	21	I	CHIP SELECT: A low on this input enables the 8254 to respond to RD and WR signals. RD and WR are ignored otherwise.		
A1, A0	20 – 9	I	ADDRESS: Used to select one of the three Counters or the Control Word Register for read or write operations. Normally connected to the system address bus.		
			A1	A0	Selects
			0	0	Counter 0
			0	1	Counter 1
			1	0	Counter 2
			1	1	Control Word Register
CLK 2	18	I	CLOCK 2: Clock input of Counter 2.		
OUT 2	17	O	OUT 2: Output of Counter 2.		

Pin Description (cont..)

GATE 2	16	I	GATE 2: Gate input of Counter 2.
CLK 1	15	I	CLOCK 1: Clock input of Counter 1.
GATE 1	14	I	GATE 1: Gate input of Counter 1.
OUT 1	OUT 1	O	OUT 1: Output of Counter 1.

Functional Description

- The 8254 is a programmable interval timer/counter designed for use with Intel microcomputer systems.
- It is a general purpose, multi-timing element that can be treated as an array of I/O ports in the system software.
- The 8254 solves one of the most common problems in any microcomputer system, the generation of accurate time delays under software control. Instead of setting up timing loops in software, the programmer configures the 8254 to match his requirements and programs one of the counters for the desired delay.

Functional Description (cont..)

- After the desired delay, the 8254 will interrupt the CPU. Software overhead is minimal and variable length delays can easily be accommodated.
- Some of the other counter/timer functions common to microcomputers which can be implemented with the 8254 are:
 - Real time clock
 - Event-counter
 - Digital one-shot

Functional Description (cont..)

- Programmable rate generator
- Square wave generator
- Binary rate multiplier
- Complex waveform generator
- Complex motor controller

Block Diagram

- **DATA BUS BUFFER:** This 3-state, bi-directional, 8-bit buffer is used to interface the 8254 to the system bus, see the figure below : Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions.
- **READ/WRITE LOGIC :** The Read/Write Logic accepts inputs from the system bus and generates control signals for the other functional blocks of the 8254. A_1 and A_0 select one of the three counters or the Control Word Register to be read from/written into.
- A “low” on the \overline{RD} input tells the 8254 that the CPU is reading one of the counters.

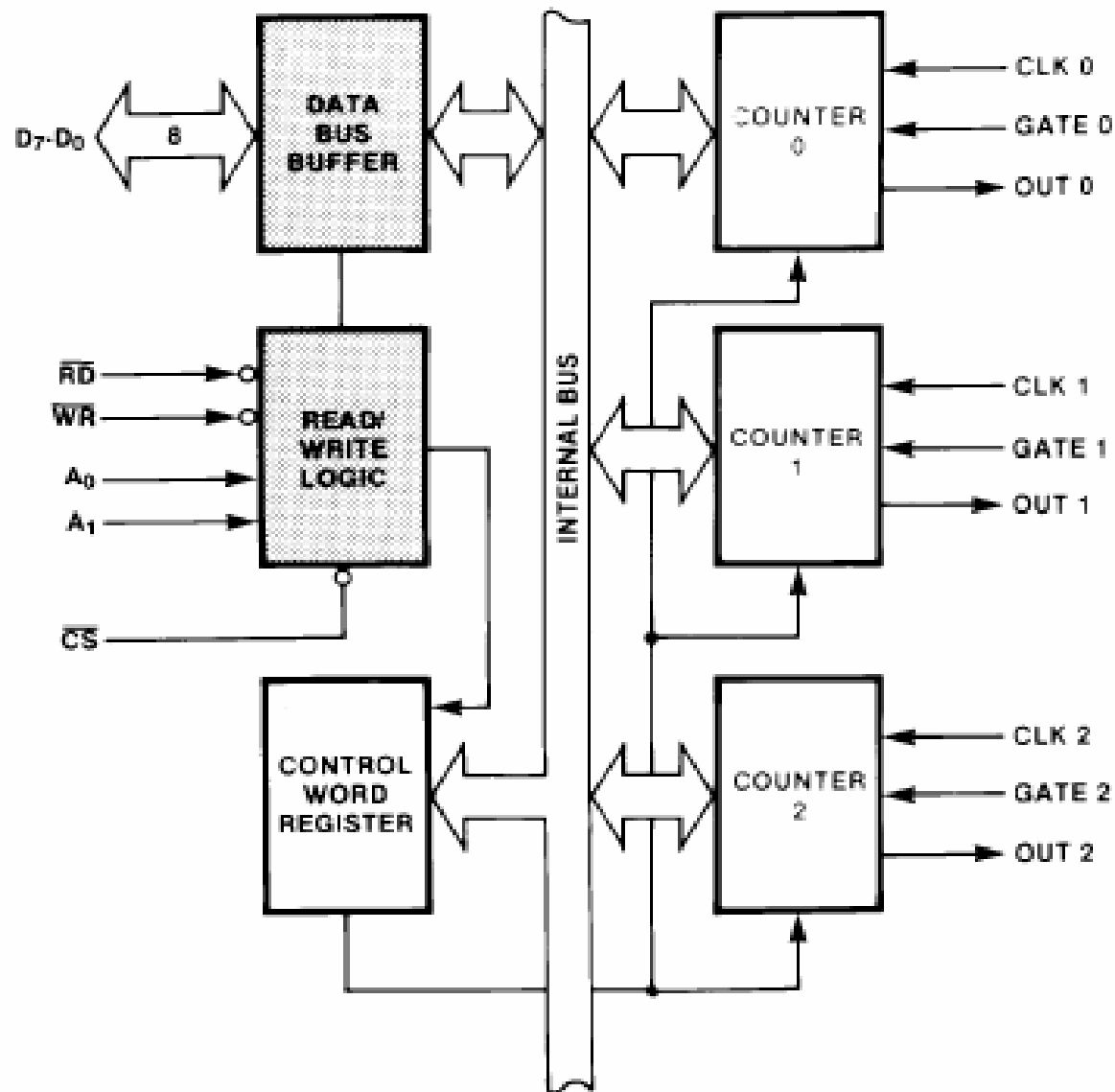


Figure 3. Block Diagram Showing Data Bus Buffer and Read/Write Logic Functions

Block Diagram (cont..)

- A “low” on the \overline{WR} input tells the 8254 that the CPU is writing either a Control Word or an initial count. Both \overline{RD} and \overline{WR} are qualified by \overline{CS} ; \overline{RD} and \overline{WR} are ignored unless the 8254 has been selected by holding \overline{CS} low.
- **CONTROL WORD REGISTER** :The Control Word Register (see Figure 4) is selected by the Read/Write Logic when $A_1, A_0 = 11$. If the CPU then does a write operation to the 8254, the data is stored in the Control Word Register and is interpreted as a Control Word used to define the operation of the Counters.

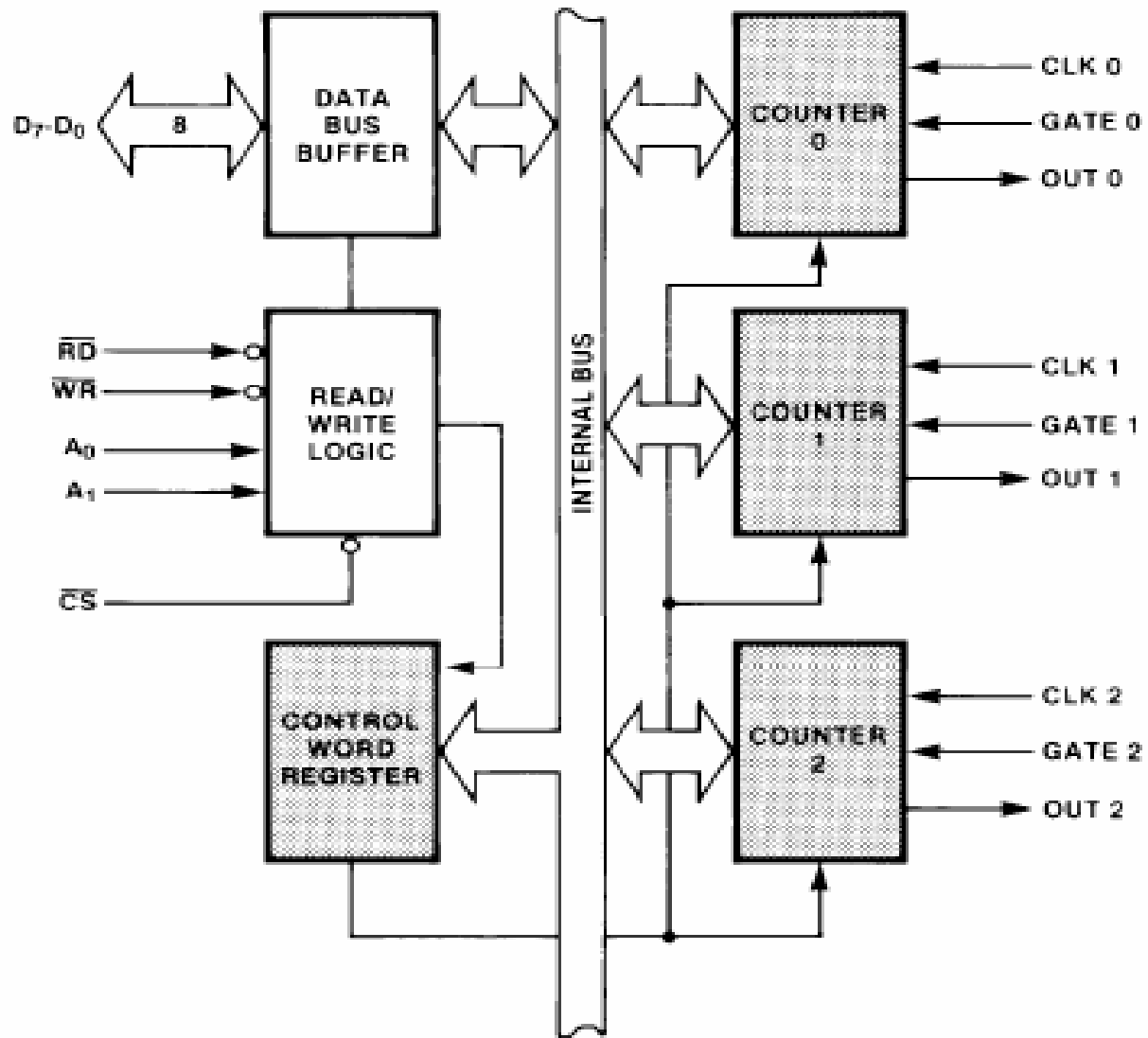


Figure 4. Block Diagram Showing Control Word Register and Counter Functions

Block Diagram (cont..)

- The Control Word Register can only be written to; status information is available with the Read-Back Command.
- **COUNTER 0, COUNTER 1, COUNTER 2** :These three functional blocks are identical in operation, so only a single Counter will be described. The internal block diagram of a single counter is shown in Figure 5.
- The Counters are fully independent. Each Counter may operate in a different Mode.
- The Control Word Register is shown in the figure; it is not part of the Counter itself, but its contents determine how the Counter operates.

Block Diagram (cont..)

- The status register, shown in Figure 5, when latched, contains the current contents of the Control Word Register and status of the output and null count flag. (See detailed explanation of the Read-Back command.)
- The actual counter is labelled CE (for "Counting Element"). It is a 16-bit presettable synchronous down counter. OLM and OLL are two 8-bit latches. OL stands for "Output Latch"; the subscripts M and L stand for "Most significant byte" and "Least significant byte" respectively.

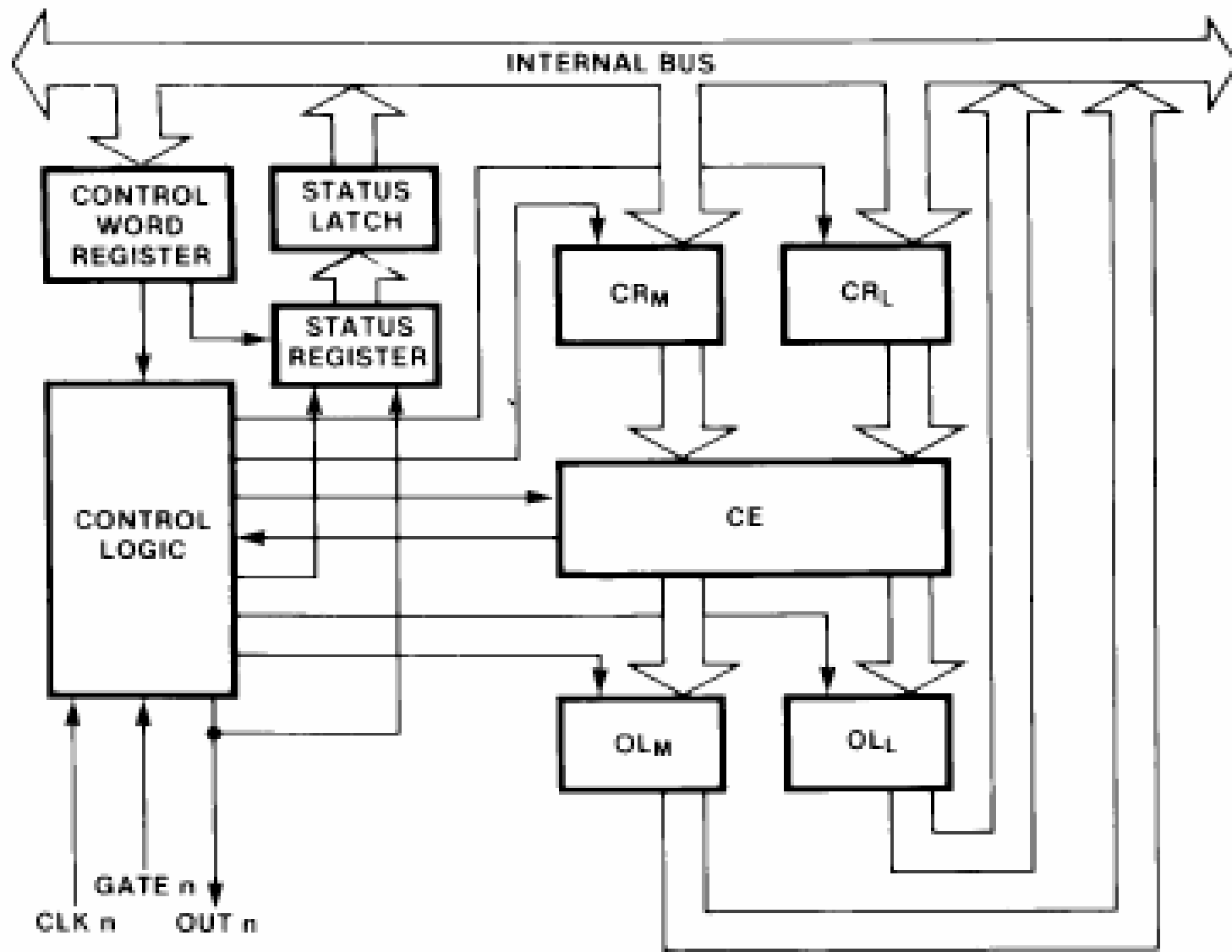


Figure 5. Internal Block Diagram of a Counter

Block Diagram (cont..)

- Both are normally referred to as one unit and called just OL. These latches normally ``follow'' the CE, but if a suitable Counter Latch Command is sent to the 8254, the latches ``latch'' the present count until read by the CPU and then return to ``following'' the CE.
- One latch at a time is enabled by the counter's Control Logic to drive the internal bus. This is how the 16-bit Counter communicates over the 8-bit internal bus. Note that the CE itself cannot be read; whenever you read the count, it is the OL that is being read.

Block Diagram (cont..)

- Similarly, there are two 8-bit registers called CRM and CRL (for ``Count Register"). Both are normally referred to as one unit and called just CR.
- When a new count is written to the Counter, the count is stored in the CR and later transferred to the CE. The Control Logic allows one register at a time to be loaded from the internal bus. Both bytes are transferred to the CE simultaneously.
- CRM and CRL are cleared when the Counter is programmed. In this way, if the Counter has been programmed for one byte counts (either most significant byte only or least significant byte only) the other byte will be zero.

Block Diagram (cont..)

- Note that the CE cannot be written into, whenever a count is written, it is written into the CR.
- The Control Logic is also shown in the diagram.
- CLK n, GATE n, and OUT n are all connected to the outside world through the Control Logic.
- **8254 SYSTEM INTERFACE** :The 8254 is a component of the Intel Microcomputer Systems and interfaces in the same manner as all other peripherals of the family.
- It is treated by the system's software as an array of peripheral I/O ports; three are counters and the fourth is a control register for MODE programming.

Block Diagram (cont..)

- Basically, the select inputs A_0, A_1 connect to the A_0, A_1 address bus signals of the CPU. The CS can be derived directly from the address bus using a linear select method. Or it can be connected to the output of a decoder, such as an Intel 8205 for larger systems.
- **Programming the 8254** :Counters are programmed by writing a Control Word and then an initial count.
- The Control Words are written into the Control Word Register, which is selected when $A_1, A_0 = 11$. The Control Word itself specifies which Counter is being programmed.

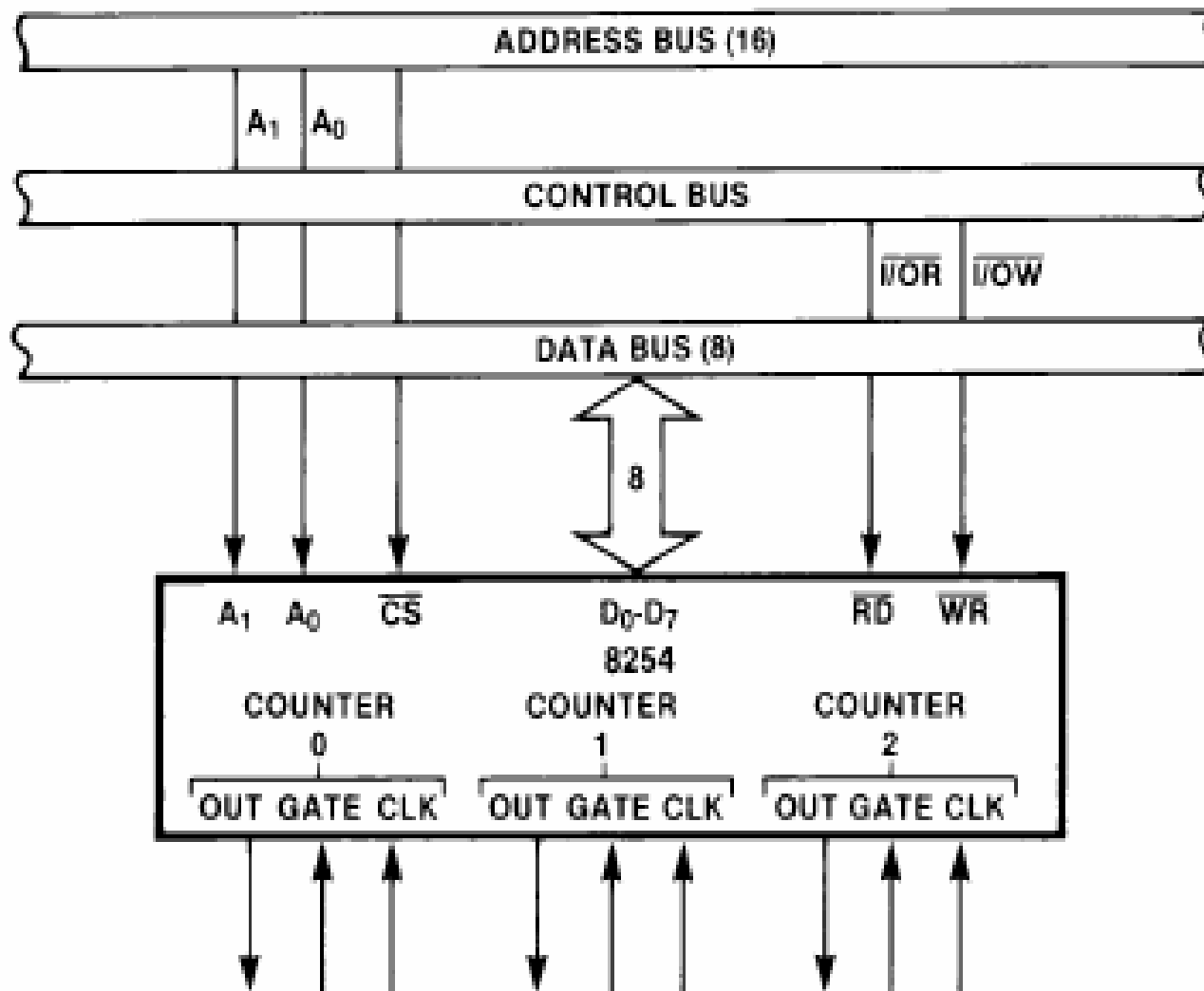


Figure 6. 8254 System Interface

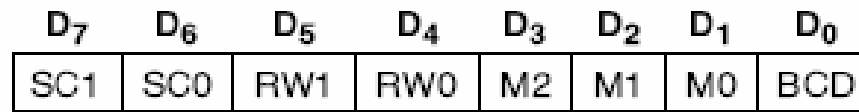
Block Diagram (cont..)

- **Control Word Format:** $A1, A0 = 11$, $CS = 0$, $\overline{RD} = 1$, $\overline{WR} = 0$.
- By contrast, initial counts are written into the Counters, not the Control Word Register. The $A1, A0$ inputs are used to select the Counter to be written into. The format of the initial count is determined by the Control Word used.
- **Write Operations:** The programming procedure for the 8254 is very flexible. Only two conventions need to be remembered:
 - 1) For each Counter, the Control Word must be written before the initial count is written.

Block Diagram (cont..)

- 2) The initial count must follow the count format specified in the Control Word (least significant byte only, most significant byte only, or least significant byte and then most significant byte).

 - Since the Control Word Register and the three Counters have separate addresses (selected by the A_1, A_0 inputs), and each Control Word specifies the Counter it applies to (SC_0, SC_1 bits), no special instruction sequence is required.
 - Any programming sequence that follows the conventions in Figure 7 is acceptable.



SC—Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Read-Back Command (see Read Operations)

M—Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

RW—Read/Write

RW1	RW0	
0	0	Counter Latch Command (see Read Operations)
0	1	Read/Write least significant byte only
1	0	Read/Write most significant byte only
1	1	Read/Write least significant byte first, then most significant byte

BCD

0	Binary Counter 16-bits
1	Binary Coded Decimal (BCD) Counter (4 Decades)

NOTE: Don't care bits (X) should be 0 to insure compatibility with future Intel products.

Figure 7. Control Word Format

Block Diagram (cont..)

- A new initial count may be written to a Counter at any time without affecting the Counter's programmed Mode in any way. Counting will be affected as described in the Mode definitions. The new count must follow the programmed count format.
- If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between writing the first and second byte to another routine which also writes into that same Counter. Otherwise, the Counter will be loaded with an incorrect count.

	A_1	A_0		A_1	A_0
Control Word—Counter 0	1	1	Control Word—Counter 2	1	1
LSB of count—Counter 0	0	0	Control Word—Counter 1	1	1
MSB of count—Counter 0	0	0	Control Word—Counter 0	1	1
Control Word—Counter 1	1	1	LSB of count—Counter 2	1	0
LSB of count—Counter 1	0	1	MSB of count—Counter 2	1	0
MSB of count—Counter 1	0	1	LSB of count—Counter 1	0	1
Control Word—Counter 2	1	1	MSB of count—Counter 1	0	1
LSB of count—Counter 2	1	0	LSB of count—Counter 0	0	0
MSB of count—Counter 2	1	0	MSB of count—Counter 0	0	0
	A_1	A_0		A_1	A_0
Control Word—Counter 0	1	1	Control Word—Counter 1	1	1
Control Word—Counter 1	1	1	Control Word—Counter 0	1	1
Control Word—Counter 2	1	1	LSB of count—Counter 1	0	1
LSB of count—Counter 2	1	0	Control Word—Counter 2	1	1
LSB of count—Counter 1	0	1	LSB of count—Counter 0	0	0
LSB of count—Counter 0	0	0	MSB of count—Counter 1	0	1
MSB of count—Counter 0	0	0	LSB of count—Counter 2	1	0
MSB of count—Counter 1	0	1	MSB of count—Counter 0	0	0
MSB of count—Counter 2	1	0	MSB of count—Counter 2	1	0

Figure 8. A Few Possible Programming Sequences

Block Diagram (cont..)

- **Read Operations:** It is often desirable to read the value of a Counter without disturbing the count in progress. This is easily done in the 8254.
- There are three possible methods for reading the counters: a simple read operation, the Counter Latch Command, and the Read-Back Command.
- Each is explained below. The first method is to perform a simple read operation. To read the Counter, which is selected with the A_1 , A_0 inputs, the CLK input of the selected Counter must be inhibited by using either the GATE input or external logic.
- Otherwise, the count may be in the process of changing when it is read, giving an undefined result.

Block Diagram (cont..)

- **COUNTER LATCH COMMAND:** The second method uses the ``Counter Latch Command".
- Like a Control Word, this command is written to the Control Word Register, which is selected when $A_1, A_0 = 11$. Also like a Control Word, the SC0, SC1 bits select one of the three Counters, but two other bits, D5 and D4, distinguish this command from a Control Word.
- The selected Counter's output latch (OL) latches the count at the time the Counter Latch Command is received. This count is held in the latch until it is read by the CPU (or until the Counter is reprogrammed).

A₁,A₀ = 11; CS = 0; RD = 1; WR = 0

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
SC1	SC0	0	0	X	X	X	X

SC1,SC0—specify counter to be latched

SC1	SC0	Counter
0	0	0
0	1	1
1	0	2
1	1	Read-Back Command

D5,D4—00 designates Counter Latch Command

X—don't care

NOTE:

Don't care bits (X) should be 0 to insure compatibility with future Intel products.

Figure 9. Counter Latching Command Format

Block Diagram (cont..)

- The count is then unlatched automatically and the OL returns to "following" the counting element (CE).
- This allows reading the contents of the Counters "on the fly" without affecting counting in progress.
- Multiple Counter Latch Commands may be used to latch more than one Counter. Each latched Counter's OL holds its count until it is read.
- Counter Latch Commands do not affect the programmed Mode of the Counter in any way.

Block Diagram (cont..)

- If a Counter is latched and then, some time later, latched again before the count is read, the second Counter Latch Command is ignored. The count read will be the count at the time the first Counter Latch Command was issued.
- With either method, the count must be read according to the programmed format; specifically, if the Counter is programmed for two byte counts, two bytes must be read. The two bytes do not have to be read one right after the other, read or write or programming operations of other Counters may be inserted between them.

Block Diagram (cont..)

- Another feature of the 8254 is that reads and writes of the same Counter may be interleaved.
- **Example:** If the Counter is programmed for two byte counts, the following sequence is valid.
 - 1) Read least significant byte.
 - 2) Write new least significant byte.
 - 3) Read most significant byte.
 - 4) Write new most significant byte.

Block Diagram (cont..)

- If a Counter is programmed to read/write two-byte counts, the following precaution applies: A program must not transfer control between reading the first and second byte to another routine which also reads from that same Counter. Otherwise, an incorrect count will be read.
- **READ-BACK COMMAND:** The third method uses the Read-Back Command. This command allows the user to check the count value, programmed Mode, and current states of the OUT pin and Null Count flag of the selected counter (s).

Block Diagram (cont..)

- The command is written into the Control Word Register and has the format shown in Figure 10. The command applies to the counters selected by setting their corresponding bits $D_3, D_2, D_1 = 1$.
- The read-back command may be used to latch multiple counter output latches (OL) by setting the COUNT bit $D_5 = 0$ and selecting the desired counter (s). This single command is functionally equivalent to several counter latch commands, one for each counter latched.

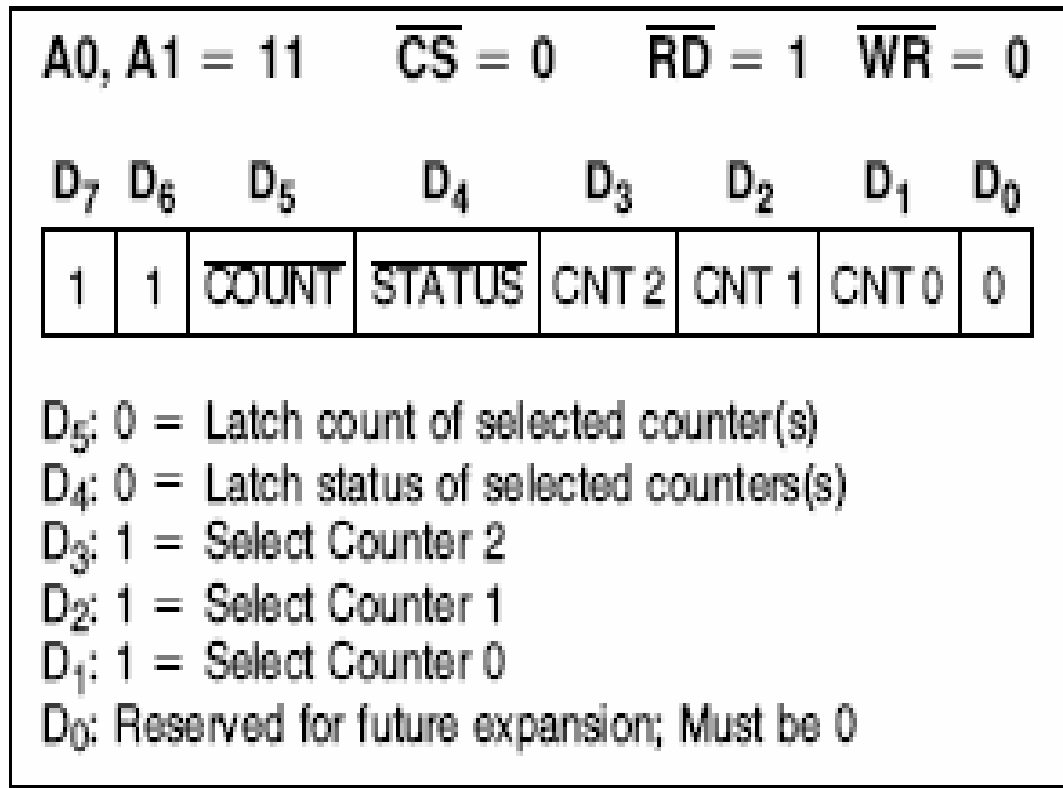


Figure 10. Read-Back Command Format

Block Diagram (cont..)

- Each counter's latched count is held until it is read (or the counter is reprogrammed).
- The counter is automatically unlatched when read, but other counters remain latched until they are read. If multiple count read-back commands are issued to the same counter without reading the count, all but the first are ignored; i.e., the count which will be read is the count at the time the first read-back command was issued.
- The read-back command may also be used to latch status information of selected counter (s) by setting STATUS bit $D_4 = 0$. Status must be latched to be read; status of a counter is accessed by a read from that counter.

Block Diagram (cont..)

- The counter status format is shown in Figure 11.
- Bits D_5 through D_0 contain the counter's programmed Mode exactly as written in the last Mode Control Word. OUTPUT bit D_7 contains the current state of the OUT pin.
- This allows the user to monitor the counter's output via software, possibly eliminating some hardware from a system. NULL COUNT bit D_6 indicates when the last count written to the counter register (CR) has been loaded into the counting element (CE).
- The exact time this happens depends on the Mode of the counter and is described in the Mode Definitions, but until the count is loaded into the counting element (CE), it can't be read from the counter.

D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
Output	Null Count	RW1	RW0	M2	M1	M0	BCD
D ₇	1 = OUT Pin is 1 0 = OUT Pin is 0						
D ₆	1 = Null Count 0 = Count available for reading						
D ₅ -D ₀	Counter programmed mode (see Figure 7)						

Figure 11. Status Byte

Block Diagram (cont..)

- If the count is latched or read before this time, the count value will not reflect the new count just written. The operation of Null Count is shown in Figure 12.
- If multiple status latch operations of the counter (s) are performed without reading the status, all but the first are ignored; i.e., the status that will be read is the status of the counter at the time the first status read-back command was issued.
- Both count and status of the selected counter (s) may be latched simultaneously by setting both COUNT and STATUS bits $D_5, D_4 = 0$. This is functionally the same as issuing two separate read-back commands at once, and the above discussions apply here also.

This Action	Causes
A. Write to the control word register; ⁽¹⁾	Null Count = 1
B. Write to the count register (CR); ⁽²⁾	Null Count = 1
C. New Count is loaded into CE (CR → CE);	Null Count = 0

NOTE:

1. Only the counter specified by the control word will have its Null Count set to 1. Null count bits of other counters are unaffected.
2. If the counter is programmed for two-byte counts (least significant byte then most significant byte) Null Count goes to 1 when the second byte is written.

Figure 12. Null Count Operation

Block Diagram (cont..)

- Specifically, if multiple count and/or status read-back commands are issued to the same counter (s) without any intervening reads, all but the first are ignored. This is illustrated in Figure 13.
- If both count and status of a counter are latched, the first read operation of that counter will return latched status, regardless of which was latched first. The next one or two reads (depending on whether the counter is programmed for one or two type counts) return latched count. Subsequent reads return unlatched count.

Command								Description	Result
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀		
1	1	0	0	0	0	1	0	Read back count and status of Counter 0	Count and status latched for Counter 0
1	1	1	0	0	1	0	0	Read back status of Counter 1	Status latched for Counter 1
1	1	1	0	1	1	0	0	Read back status of Counters 2, 1	Status latched for Counter 2, but not Counter 1
1	1	0	1	1	0	0	0	Read back count of Counter 2	Count latched for Counter 2
1	1	0	0	0	1	0	0	Read back count and status of Counter 1	Count latched for Counter 1, but not status
1	1	1	0	0	0	1	0	Read back status of Counter 1	Command ignored, status already latched for Counter 1

Figure 13. Read-Back Command Example

\overline{CS}	\overline{RD}	\overline{WR}	A_1	A_0	
0	1	0	0	0	Write into Counter 0
0	1	0	0	1	Write into Counter 1
0	1	0	1	0	Write into Counter 2
0	1	0	1	1	Write Control Word
0	0	1	0	0	Read from Counter 0
0	0	1	0	1	Read from Counter 1
0	0	1	1	0	Read from Counter 2
0	0	1	1	1	No-Operation (3-State)
1	X	X	X	X	No-Operation (3-State)
0	1	1	X	X	No-Operation (3-State)

Figure 14. Read/Write Operations Summary

Modes (cont..)

- **Mode Definitions** :The following are defined for use in describing the operation of the 8254.
- **CLK Pulse**: A rising edge, then a falling edge, in that order, of a Counter's CLK input.
- **Trigger**: A rising edge of a Counter's GATE input.
- **Counter loading**: The transfer of a count from the CR to the CE (refer to the ``Functional Description").
- **MODE 0: INTERRUPT ON TERMINAL COUNT** : Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero.

Modes (cont..)

- OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.
- GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT.
- After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N a 1 CLK pulses after the initial count is written.
- If a new count is written to the Counter, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:

Modes (cont..)

- 1) Writing the first byte disables counting. OUT is set low immediately (no clock pulse required).
- 2) Writing the second byte allows the new count to be loaded on the next CLK pulse.
 - This allows the counting sequence to be synchronized by software. Again, OUT does not go high until $N+1$ CLK pulses after the new count of N is written.
 - If an initial count is written while GATE = 0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulses later; no CLK pulse is needed to load the Counter as this has already been done.

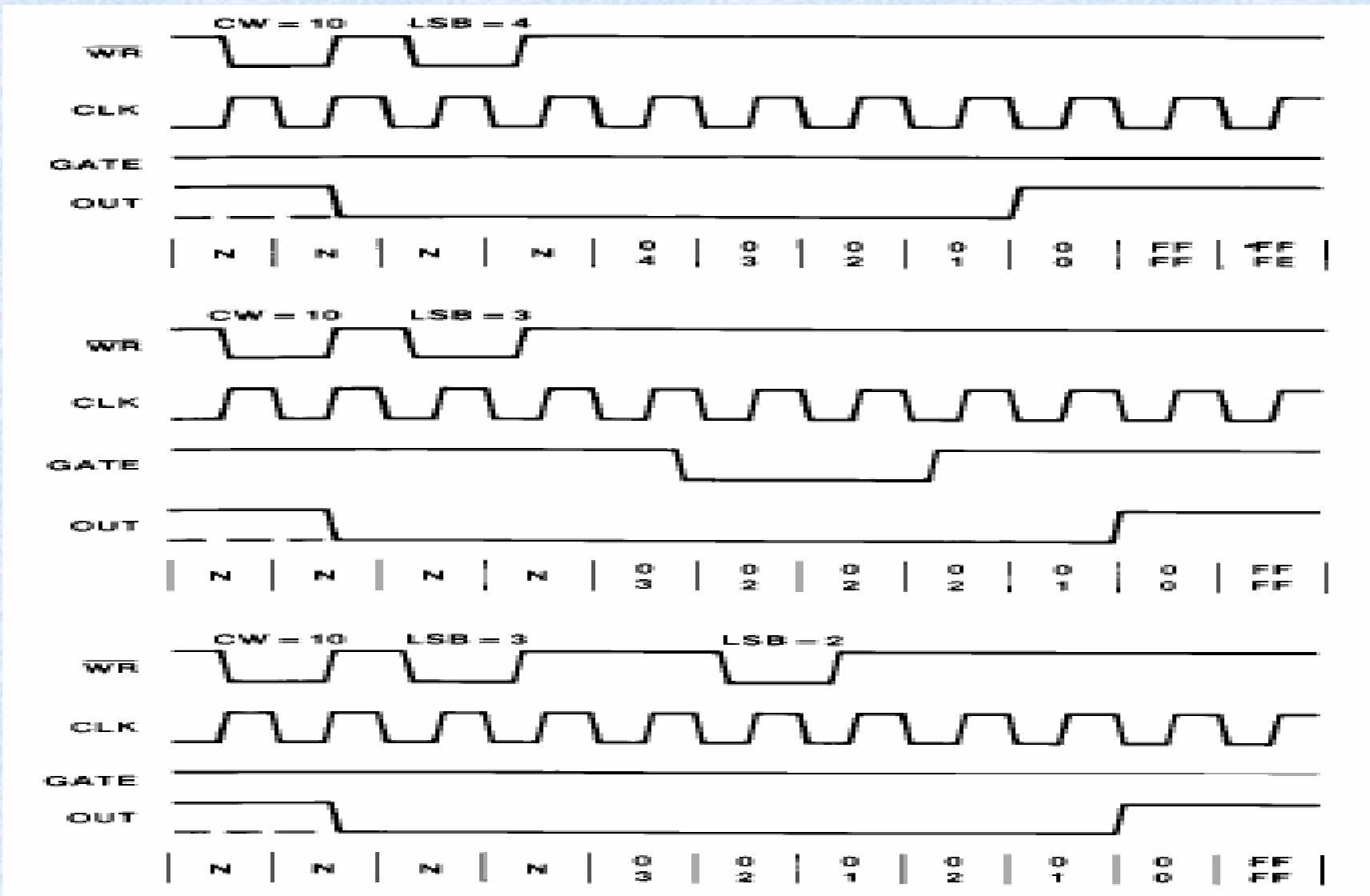


Figure 15. Mode 0

Modes (cont..)

Note:

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.
2. The counter is always selected (CS always low).
3. CW stands for ``Control Word"; CW = 10 means a control word of 10 HEX is written to the counter.
4. LSB stands for ``Least Significant Byte" of count.
5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte. Since the counter is programmed to read/write LSB only, the most significant byte cannot be read. N stands for an undefined count. Vertical lines show transitions between count values.

Modes (cont..)

- **MODE 1: *HARDWARE RETRIGGERABLE ONE-SHOT***: OUT will be initially high.
- OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero.
- OUT will then go high and remain high until the CLK pulse after the next trigger.
- After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse. An initial count of N will result in a one-shot pulse N CLK cycles in duration.

Modes (cont..)

- The one-shot is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.
- If a new count is written to the Counter during a oneshot pulse, the current one-shot is not affected unless the counter is retriggered. In that case, the Counter is loaded with the new count and the oneshot pulse continues until the new count expires.

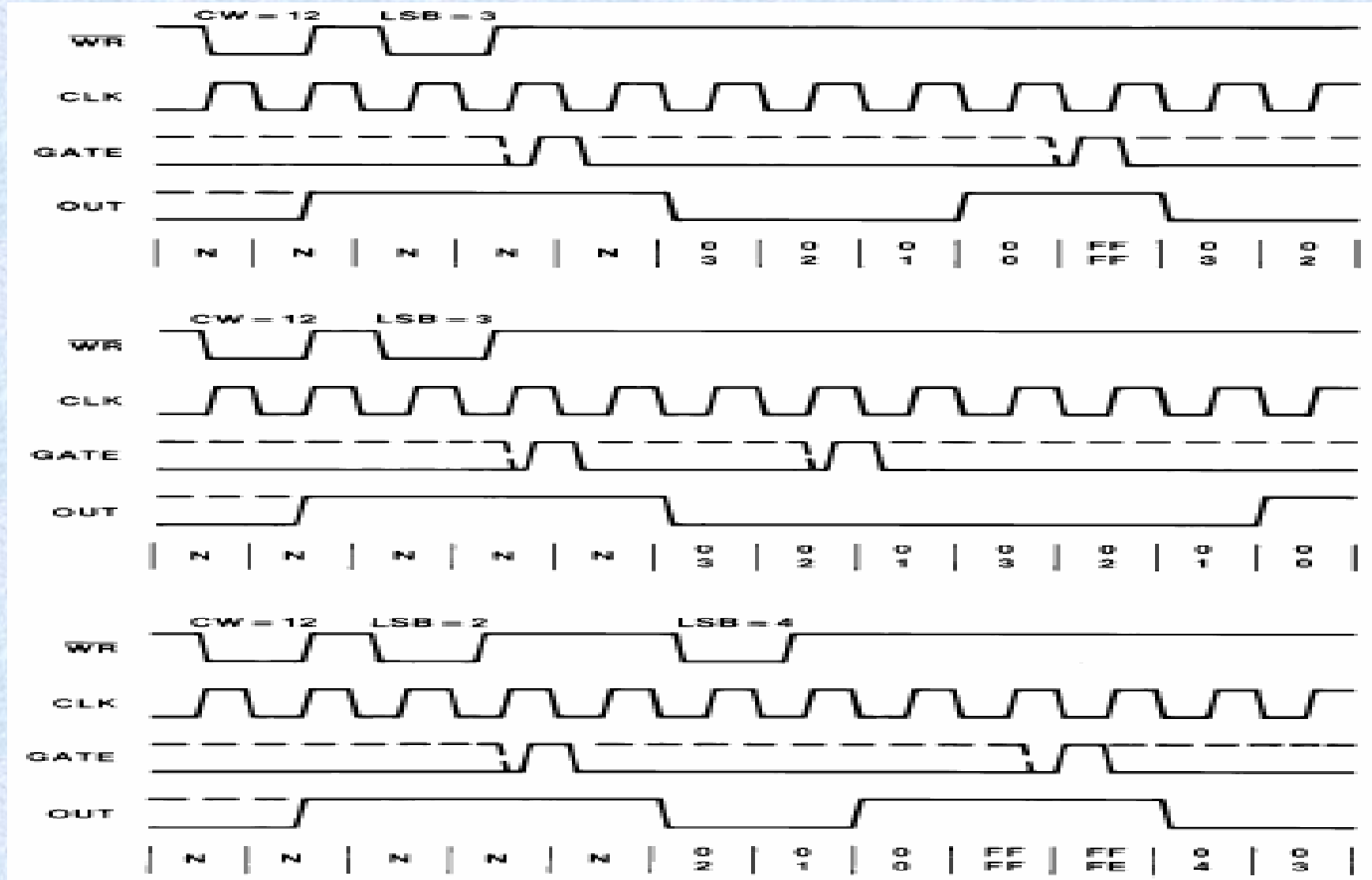


Figure 16. Mode 1

Modes (cont..)

- **MODE 2: RATE GENERATOR:** This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt.
- OUT will initially be high. When the initial count has decremented to 1, OUT goes low for one CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated.
- Mode 2 is periodic, the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.
- GATE = 1 enables counting; GATE = 0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately.

Modes (cont..)

- A trigger reloads the Counter with the initial count on the next CLK pulse, OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.
- After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK Pulses after the initial count is written.
- This allows the Counter to be synchronized by software also. Writing a new count while counting does not affect the current counting sequence.

Modes (cont..)

- If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count.
- Otherwise, the new count will be loaded at the end of the current counting cycle. In mode 2, a COUNT of 1 is illegal.
- **MODE 3: SQUARE WAVE MODE** :Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high.

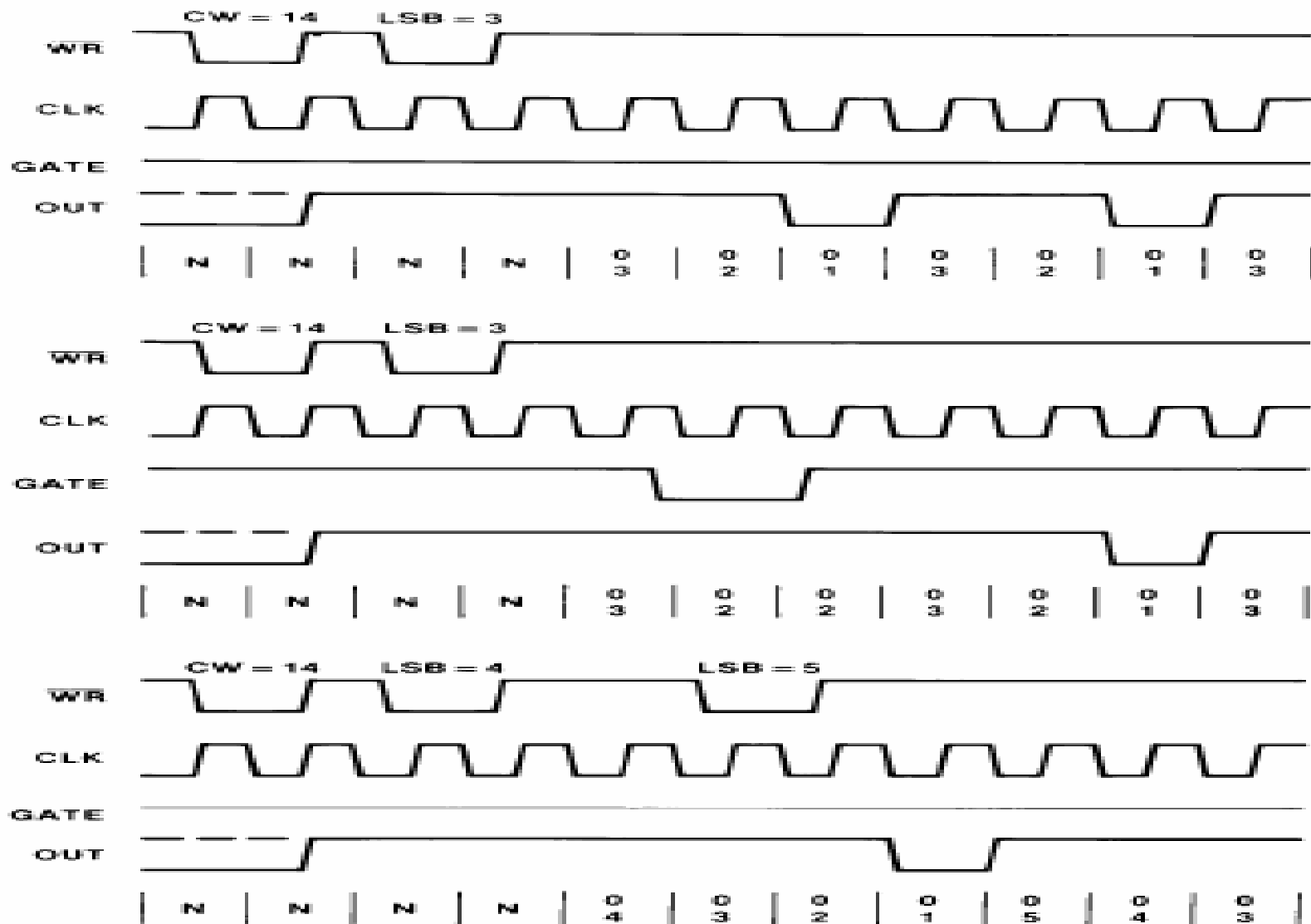


Figure 17. Mode 2

Modes (cont..)

- When half the initial count has expired, OUT goes low for the remainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely.
- An initial count of N results in a square wave with a period of N CLK cycles. $GATE = 1$ enables counting; $GATE = 0$ disables counting. If $GATE$ goes low while OUT is low, OUT is set high immediately; no CLK pulse is required.
- A trigger reloads the Counter with the initial count on the next CLK pulse. Thus the $GATE$ input can be used to synchronize the Counter.

Modes (cont..)

- After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.
- Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current half-cycle.

Modes (cont..)

- **Mode 3:Even counts:** OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses.
- When the count expires OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.
- **Odd counts:** OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses.

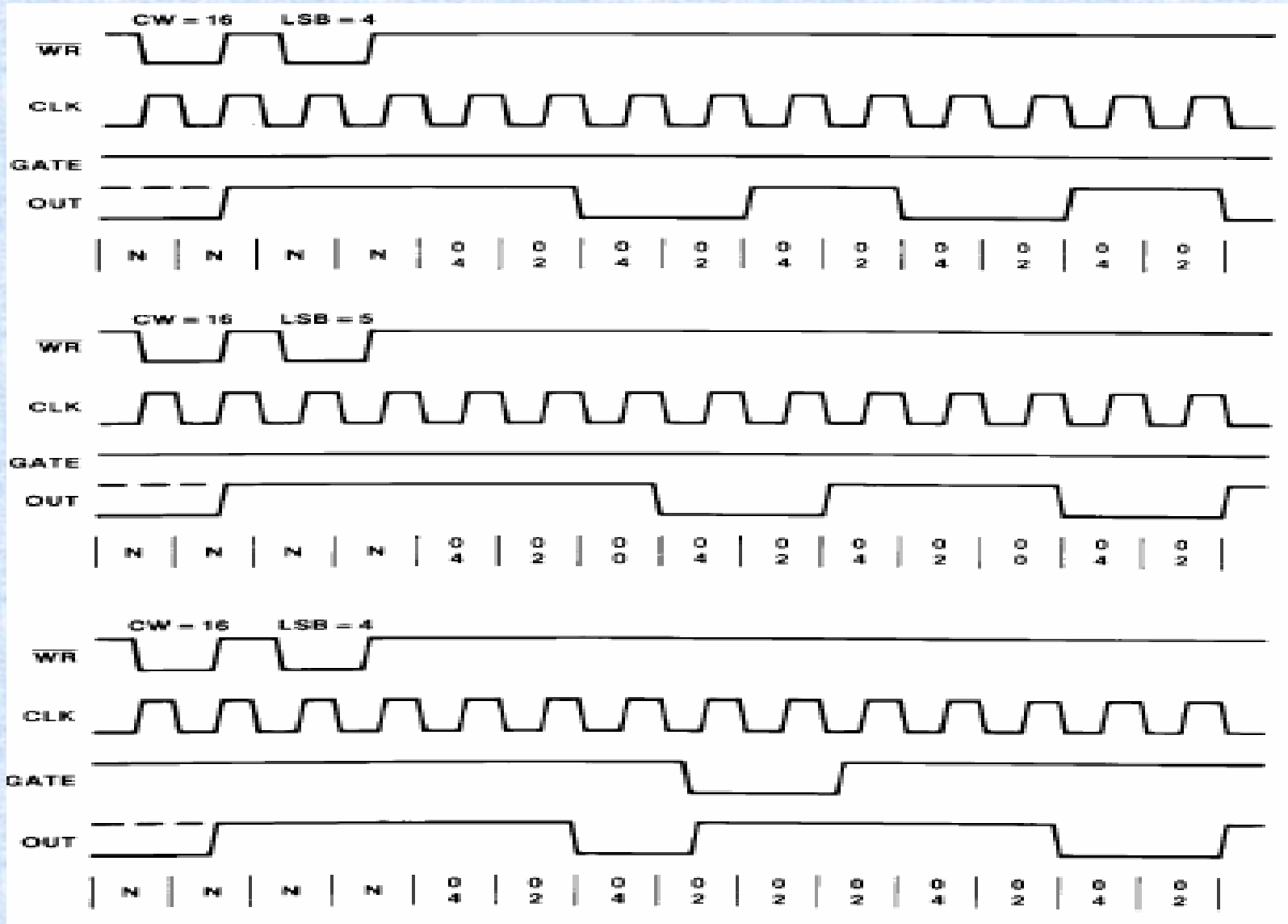


Figure 18. Mode 3

Modes (cont..)

- One CLK pulse after the count expires, OUT goes low and the Counter is reloaded with the initial count minus one.
- Succeeding CLK pulses decrement the count by two.
- When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely.
- So for odd counts, OUT will be high for $(N - 1)/2$ counts and low for $(N - 1)/2$ counts.

Modes (cont..)

- **MODE 4: SOFTWARE TRIGGERED STROBE :**
- OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is ``triggered`` by writing the initial count.
- GATE = 1 enables counting; GATE = 0 disables counting. GATE has no effect on OUT. After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse.
- This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until $N + 1$ CLK pulses after the initial count is written.

Modes (cont..)

- If a new count is written during counting, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:
 - 1) Writing the first byte has no effect on counting.
 - 2) Writing the second byte allows the new count to be loaded on the next CLK pulse.
- This allows the sequence to be ``retriggered" by software. OUT strobes low N a 1 CLK pulses after the new count of N is written.

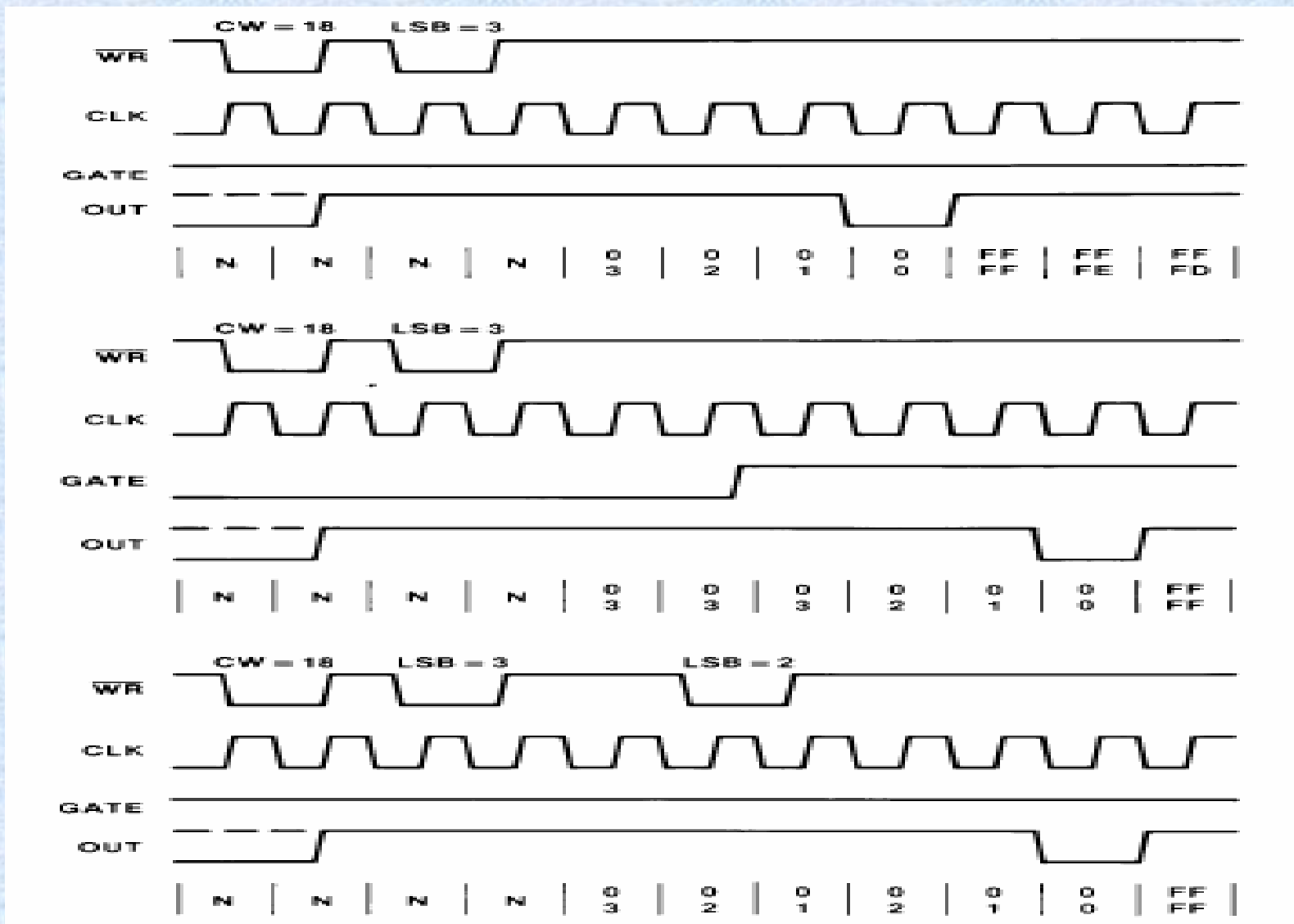


Figure 19. Mode 4

Modes (cont..)

- **MODE 5: HARDWARE TRIGGERED STROBE (RETRIGGERABLE)** :OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.
- After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until $N = 1$ CLK pulses after a trigger.

Modes (cont..)

- A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable. OUT will not strobe low for $N + 1$ CLK pulses after any trigger. GATE has no effect on OUT.
- If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

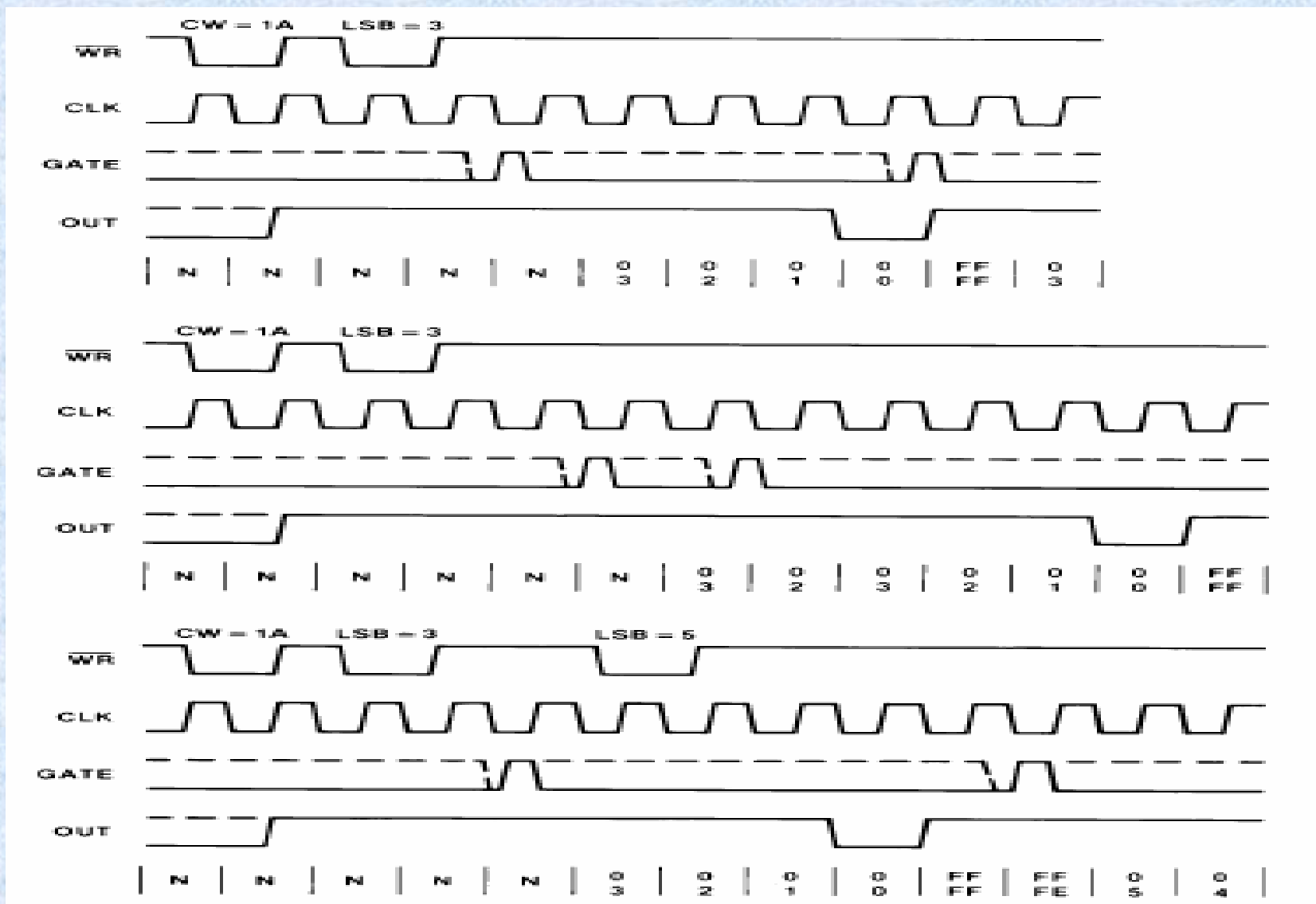


Figure 20. Mode 5

Modes (cont..)

- **Operation Common to All Modes:**
- **PROGRAMMING:** When a Control Word is written to a Counter, all Control Logic is immediately reset and OUT goes to a known initial state; no CLK pulses are required for this.
- **GATE:** The GATE input is always sampled on the rising edge of CLK. In Modes 0, 2, 3, and 4 the GATE input is level sensitive, and the logic level is sampled on the rising edge of CLK. In Modes 1, 2, 3, and 5 the GATE input is rising-edge sensitive.

Modes (cont..)

- In these Modes, a rising edge of GATE (trigger) sets an edge-sensitive flip-flop in the Counter. This flip-flop is then sampled on the next rising edge of CLK; the flip-flop is reset immediately after it is sampled. In this way, a trigger will be detected no matter when it occurs—a high logic level does not have to be maintained until the next rising edge of CLK.
- Note that in Modes 2 and 3, the GATE input is both edge- and level-sensitive. In Modes 2 and 3, if a CLK source other than the system clock is used, GATE should be pulsed immediately following WR of a new count value.

Signal Status Modes	Low Or Going Low	Rising	High
0	Disables Counting	— —	Enables Counting
1	— —	1) Initiates Counting 2) Resets Output after Next Clock	— —
2	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
3	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
4	Disables Counting	— —	Enables Counting
5	— —	Initiates Counting	— —

Figure 21. Gate Pin Operations Summary

Modes (cont..)

- **COUNTER:** New counts are loaded and Counters are decremented on the falling edge of CLK.
- The largest possible initial count is 0, this is equivalent to 2^{16} for binary counting and 10^4 for BCD counting. The Counter does not stop when it reaches zero.
- In Modes 0, 1, 4, and 5 the Counter ``wraps around" to the highest count, either FFFF hex for binary counting or 9999 for BCD counting and continues counting.
- Modes 2 and 3 are periodic; the Counter reloads itself with the initial count and continues counting from there.

Mode	Min Count	Max Count
0	1	0
1	1	0
2	2	0
3	2	0
4	1	0
5	1	0

NOTE: 0 is equivalent to 2^{16} for binary counting and 10^4 for BCD counting.

Figure 22. Minimum and Maximum Initial Counts