

PIO 8255 (cont..)

- The parallel input-output port chip 8255 is also called as programmable *peripheral input-output port*. The Intel's 8255 is designed for use with Intel's 8-bit, 16-bit and higher capability microprocessors. It has 24 input/output lines which may be individually programmed in two groups of twelve lines each, or three groups of eight lines. The two groups of I/O pins are named as Group A and Group B. Each of these two groups contains a subgroup of eight I/O lines called as 8-bit port and another subgroup of four lines or a 4-bit port. Thus Group A contains an 8-bit port A along with a 4-bit port. C upper.

PIO 8255 (cont..)

- The port A lines are identified by symbols PA_0 - PA_7 while the port C lines are identified as PC_4 - PC_7 . Similarly, Group B contains an 8-bit port B, containing lines PB_0 - PB_7 and a 4-bit port C with lower bits PC_0 - PC_3 . The port C upper and port C lower can be used in combination as an 8-bit port C.
- Both the port C are assigned the same address. Thus one may have either three 8-bit I/O ports or two 8-bit and two 4-bit ports from 8255. All of these ports can function independently either as input or as output ports. This can be achieved by programming the bits of an internal register of 8255 called as control word register (CWR).

PIO 8255 (cont..)

- The internal block diagram and the pin configuration of 8255 are shown in fig.
- The 8-bit data bus buffer is controlled by the read/write control logic. The read/write control logic manages all of the internal and external transfers of both data and control words.
- \overline{RD} , \overline{WR} , A_1 , A_0 and RESET are the inputs provided by the microprocessor to the READ/ WRITE control logic of 8255. The 8-bit, 3-state bidirectional buffer is used to interface the 8255 internal data bus with the external system data bus.

PIO 8255 (cont..)

- This buffer receives or transmits data upon the execution of input or output instructions by the microprocessor. The control words or status information is also transferred through the buffer.
- The signal description of 8255 are briefly presented as follows :
- **PA₇-PA₀**: These are eight port A lines that acts as either latched output or buffered input lines depending upon the control word loaded into the control word register.
- **PC₇-PC₄** : Upper nibble of port C lines. They may act as either output latches or input buffers lines.

PIO 8255 (cont..)

- This port also can be used for generation of handshake lines in mode 1 or mode 2.
- **PC₃-PC₀** : These are the lower port C lines, other details are the same as PC₇-PC₄ lines.
- **PB₀-PB₇** : These are the eight port B lines which are used as latched output lines or buffered input lines in the same way as port A.
- **$\overline{\text{RD}}$** : This is the input line driven by the microprocessor and should be low to indicate read operation to 8255.
- **$\overline{\text{WR}}$** : This is an input line driven by the microprocessor. A low on this line indicates write operation.

PIO 8255 (cont..)

- $\overline{\text{CS}}$: This is a chip select line. If this line goes low, it enables the 8255 to respond to $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals, otherwise $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signal are neglected.
- $\text{A}_1\text{-A}_0$: These are the address input lines and are driven by the microprocessor. These lines $\text{A}_1\text{-A}_0$ with $\overline{\text{RD}}$, $\overline{\text{WR}}$ and $\overline{\text{CS}}$ from the following operations for 8255. These address lines are used for addressing any one of the four registers, i.e. three ports and a control word register as given in table below.
- In case of 8086 systems, if the 8255 is to be interfaced with lower order data bus, the A_0 and A_1 pins of 8255 are connected with A_1 and A_2 respectively.

$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{CS}}$	A_1	A_0	Input (Read) cycle
0	1	0	0	0	Port A to Data bus
0	1	0	0	1	Port B to Data bus
0	1	0	1	0	Port C to Data bus
0	1	0	1	1	CWR to Data bus

$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{CS}}$	A_1	A_0	Output (Write) cycle
1	0	0	0	0	Data bus to Port A
1	0	0	0	1	Data bus to Port B
1	0	0	1	0	Data bus to Port C
1	0	0	1	1	Data bus to CWR

$\overline{\text{RD}}$	$\overline{\text{WR}}$	$\overline{\text{CS}}$	A_1	A_0	Function
X	X	1	X	X	Data bus tristated
1	1	0	X	X	Data bus tristated

Control Word Register

PIO 8255.

- **D₀-D₇** : These are the data bus lines those carry data or control word to/from the microprocessor.
- **RESET** : A logic high on this line clears the control word register of 8255. All ports are set as input ports by default after reset.

Block Diagram of 8255 (Architecture)

(cont..)

- It has a 40 pins of 4 groups.
 1. Data bus buffer
 2. Read Write control logic
 3. Group A and Group B controls
 4. Port A, B and C
- ***Data bus buffer***: This is a tristate bidirectional buffer used to interface the 8255 to system databus. Data is transmitted or received by the buffer on execution of input or output instruction by the CPU.
- Control word and status information are also transferred through this unit.

Block Diagram of 8255 (Architecture)

(cont..)

- ***Read/Write control logic:*** This unit accepts control signals (\overline{RD} , \overline{WR}) and also inputs from address bus and issues commands to individual group of control blocks (Group A, Group B).
- It has the following pins.
 - a) \overline{CS} – Chipselect : A low on this PIN enables the communication between CPU and 8255.
 - b) \overline{RD} (Read) – A low on this pin enables the CPU to read the data in the ports or the status word through data bus buffer.

Block Diagram of 8255 (Architecture)

(cont..)

- c) **\overline{WR}** (Write) : A low on this pin, the CPU can write data on to the ports or on to the control register through the data bus buffer.
- d) **RESET**: A high on this pin clears the control register and all ports are set to the input mode
- e) **A_0 and A_1** (Address pins) : These pins in conjunction with \overline{RD} and \overline{WR} pins control the selection of one of the 3 ports.
 - ***Group A and Group B controls*** : These block receive control from the CPU and issues commands to their respective ports.

Block Diagram of 8255 (Architecture)

(cont..)

- Group A - PA and PCU ($PC_7 - PC_4$)
- Group B - PCL ($PC_3 - PC_0$)
- Control word register can only be written into no read operation of the CW register is allowed.
- a) **Port A**: This has an 8 bit latched/buffered O/P and 8 bit input latch. It can be programmed in 3 modes – mode 0, mode 1, mode 2.
 - b) **Port B**: This has an 8 bit latched / buffered O/P and 8 bit input latch. It can be programmed in mode 0, mode 1.

Block Diagram of 8255 (Architecture).

c) **Port C** : This has an 8 bit latched input buffer and 8 bit output latched/buffer. This port can be divided into two 4 bit ports and can be used as control signals for port A and port B. it can be programmed in mode 0.

Modes of Operation of 8255 (cont..)

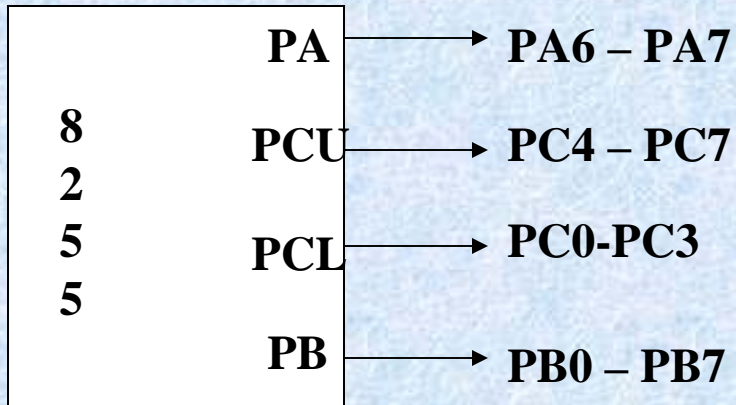
- These are two basic modes of operation of 8255. I/O mode and Bit Set-Reset mode (BSR).
- In I/O mode, the 8255 ports work as programmable I/O ports, while in BSR mode only port C (PC_0 - PC_7) can be used to set or reset its individual port bits.
- Under the I/O mode of operation, further there are three modes of operation of 8255, so as to support different types of applications, mode 0, mode 1 and mode 2.

Modes of Operation of 8255 (cont..)

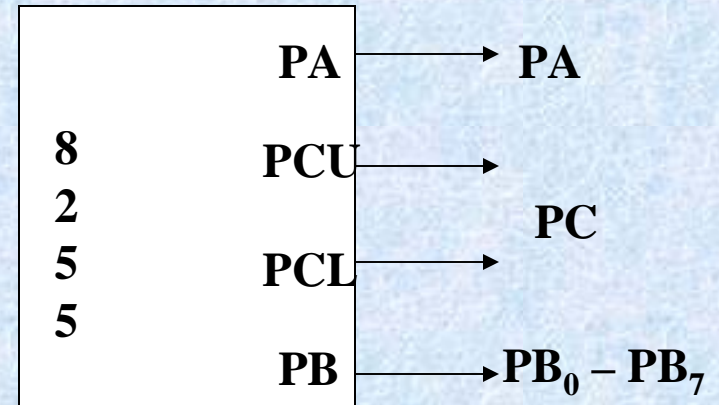
- ***BSR Mode***: In this mode any of the 8-bits of port C can be set or reset depending on D_0 of the control word. The bit to be set or reset is selected by bit select flags D_3 , D_2 and D_1 of the CWR as given in table.
- **I/O Modes :**
 - a) ***Mode 0 (Basic I/O mode)***: This mode is also called as basic input/output mode. This mode provides simple input and output capabilities using each of the three ports. Data can be simply read from and written to the input and output ports respectively, after appropriate initialisation.

D₃	D₂	D₁	Selected bits of port C
0	0	0	D₀
0	0	1	D₁
0	1	0	D₂
0	1	1	D₃
1	0	0	D₄
1	0	1	D₅
1	1	0	D₆
1	1	1	D₇

BSR Mode : CWR Format



All Output



Port A and Port C acting as O/P. Port B acting as I/P

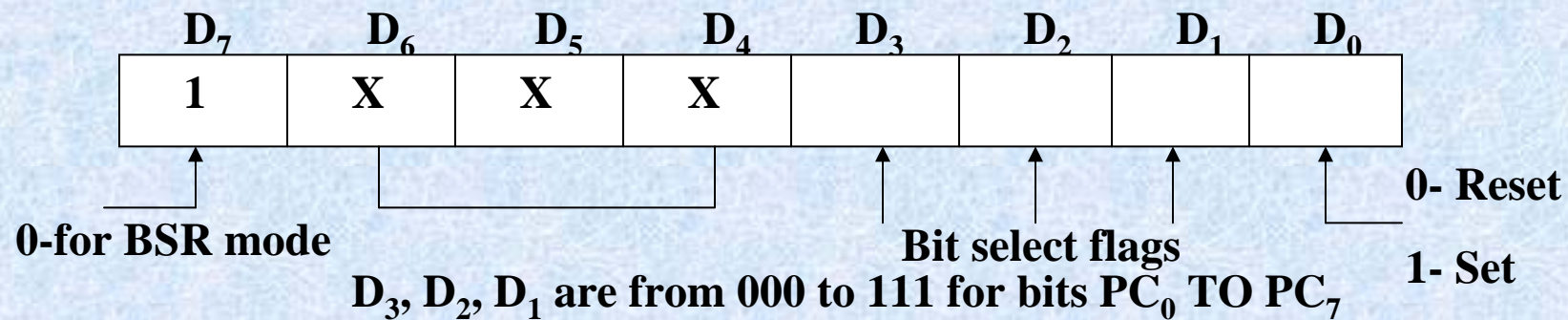
Mode 0

Modes of Operation of 8255 (cont..)

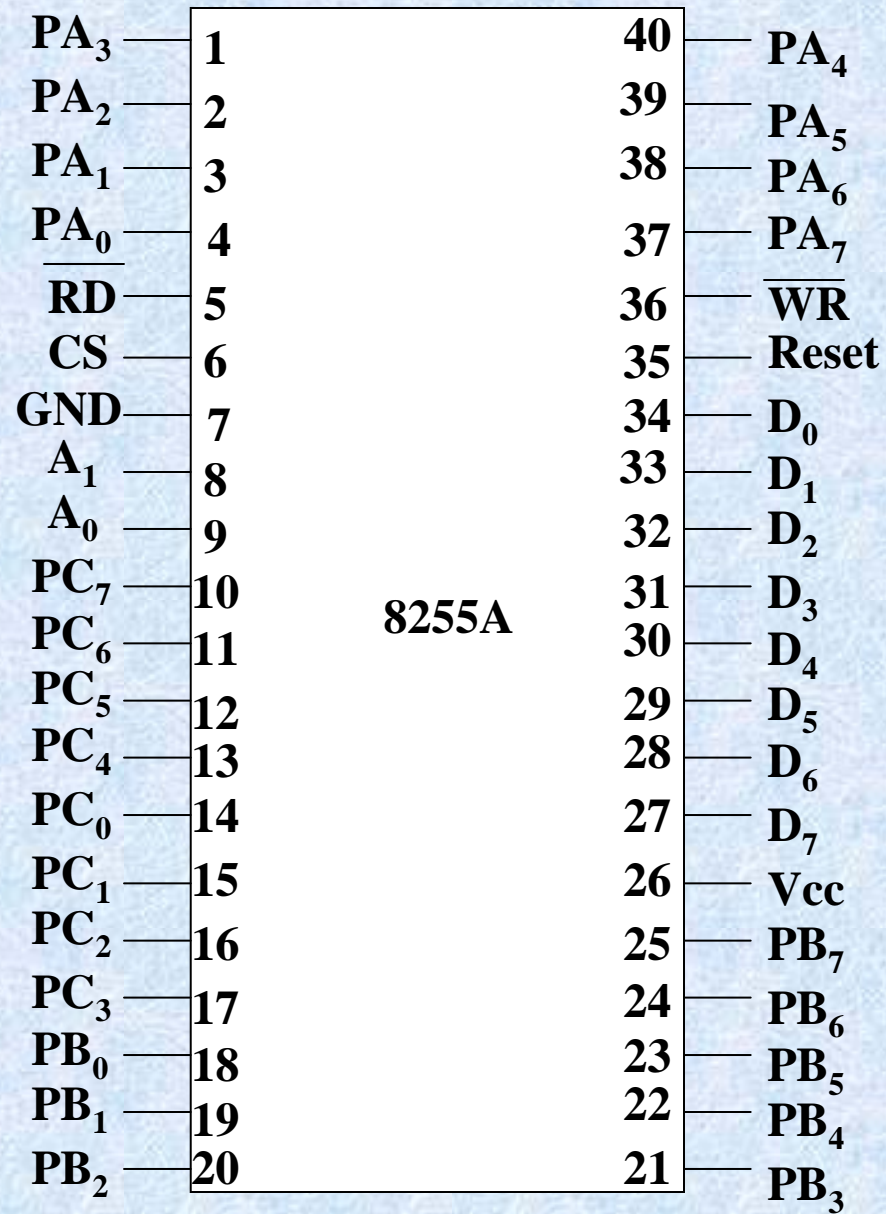
- The salient features of this mode are as listed below:
 1. Two 8-bit ports (port A and port B)and two 4-bit ports (port C upper and lower) are available. The two 4-bit ports can be combinedly used as a third 8-bit port.
 2. Any port can be used as an input or output port.
 3. Output ports are latched. Input ports are not latched.
 4. A maximum of four ports are available so that overall 16 I/O configuration are possible.
- All these modes can be selected by programming a register internal to 8255 known as CWR.

Modes of Operation of 8255 (cont..)

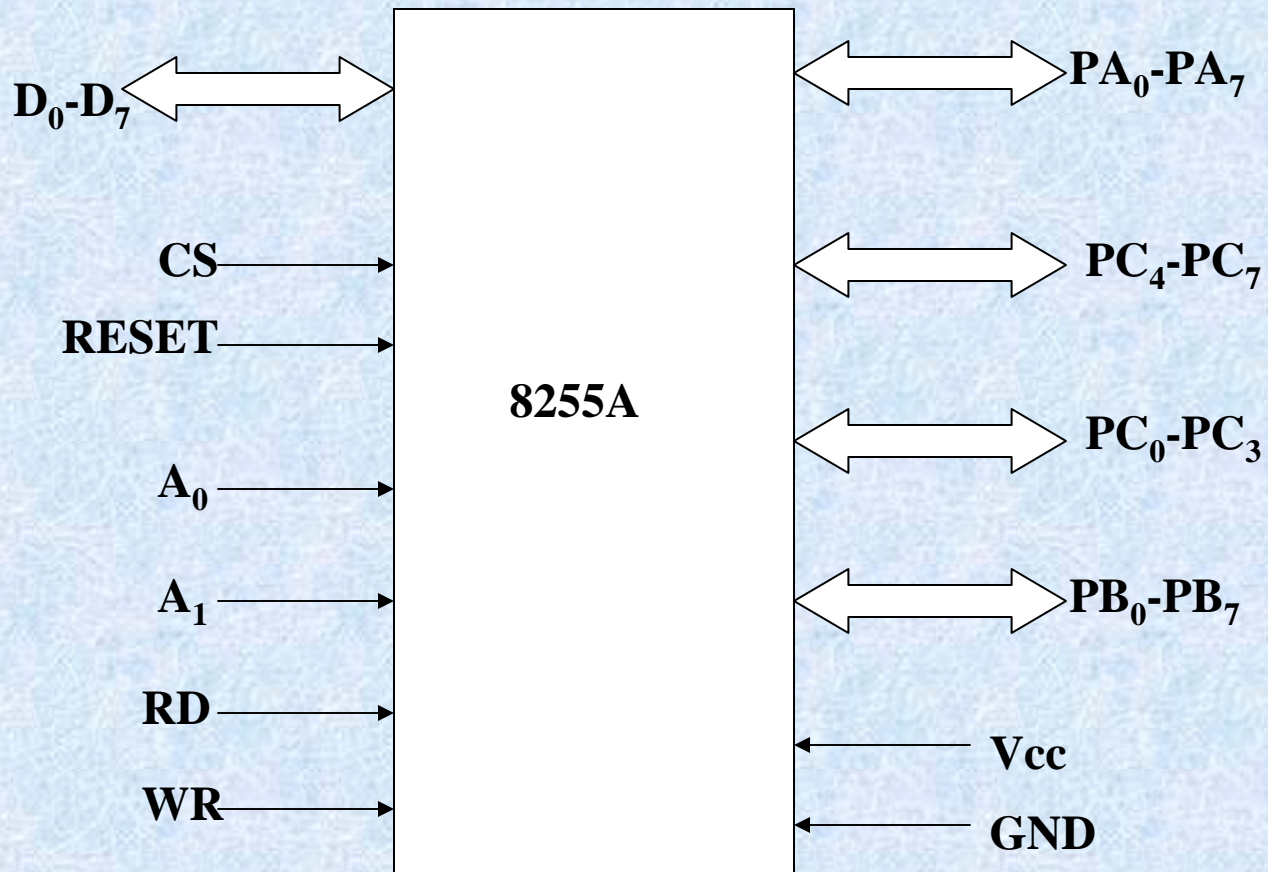
- The control word register has two formats. The first format is valid for I/O modes of operation, i.e. modes 0, mode 1 and mode 2 while the second format is valid for bit set/reset (BSR) mode of operation. These formats are shown in following fig.



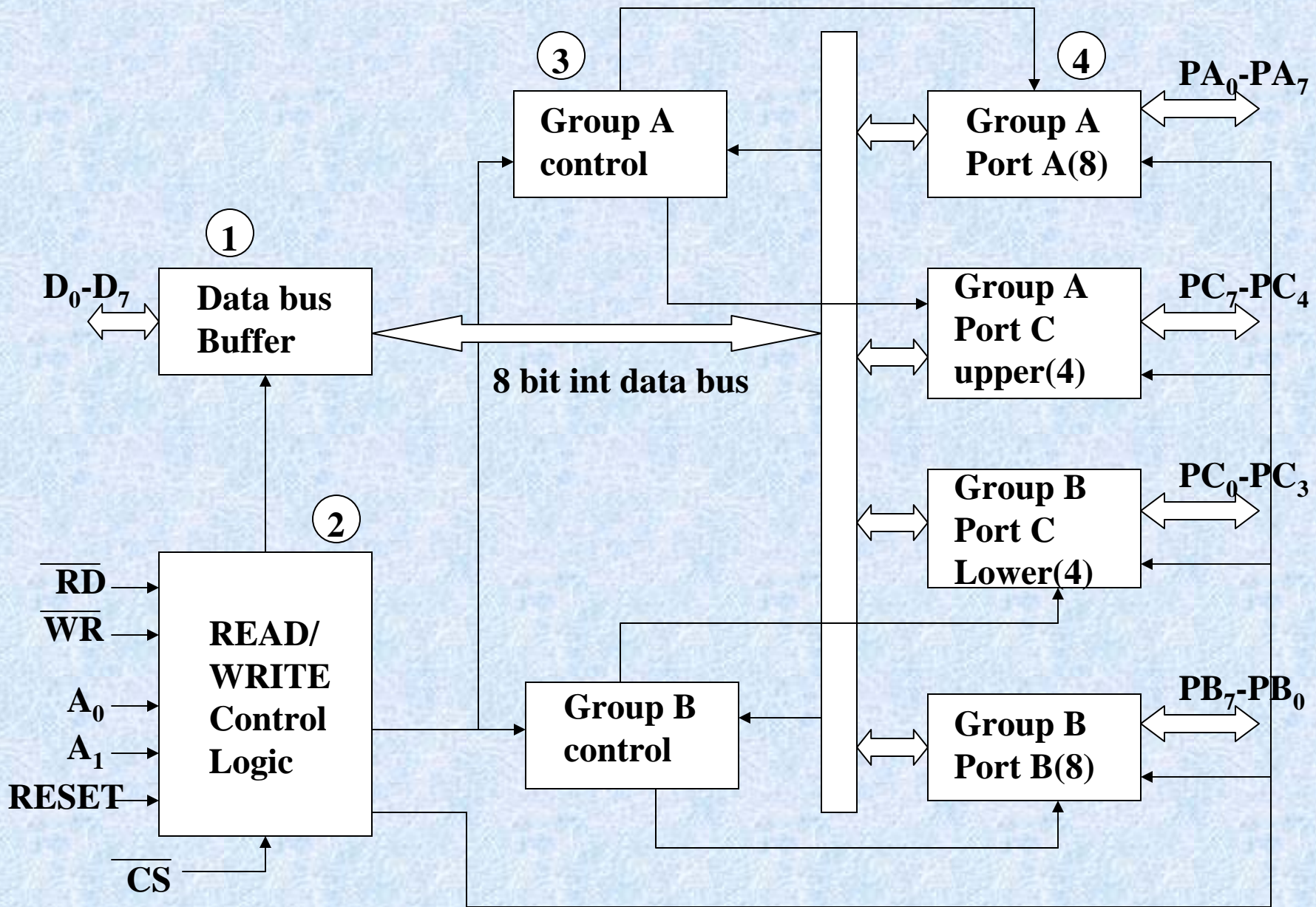
**I/O Mode Control Word Register Format and
BSR Mode Control Word Register Format**



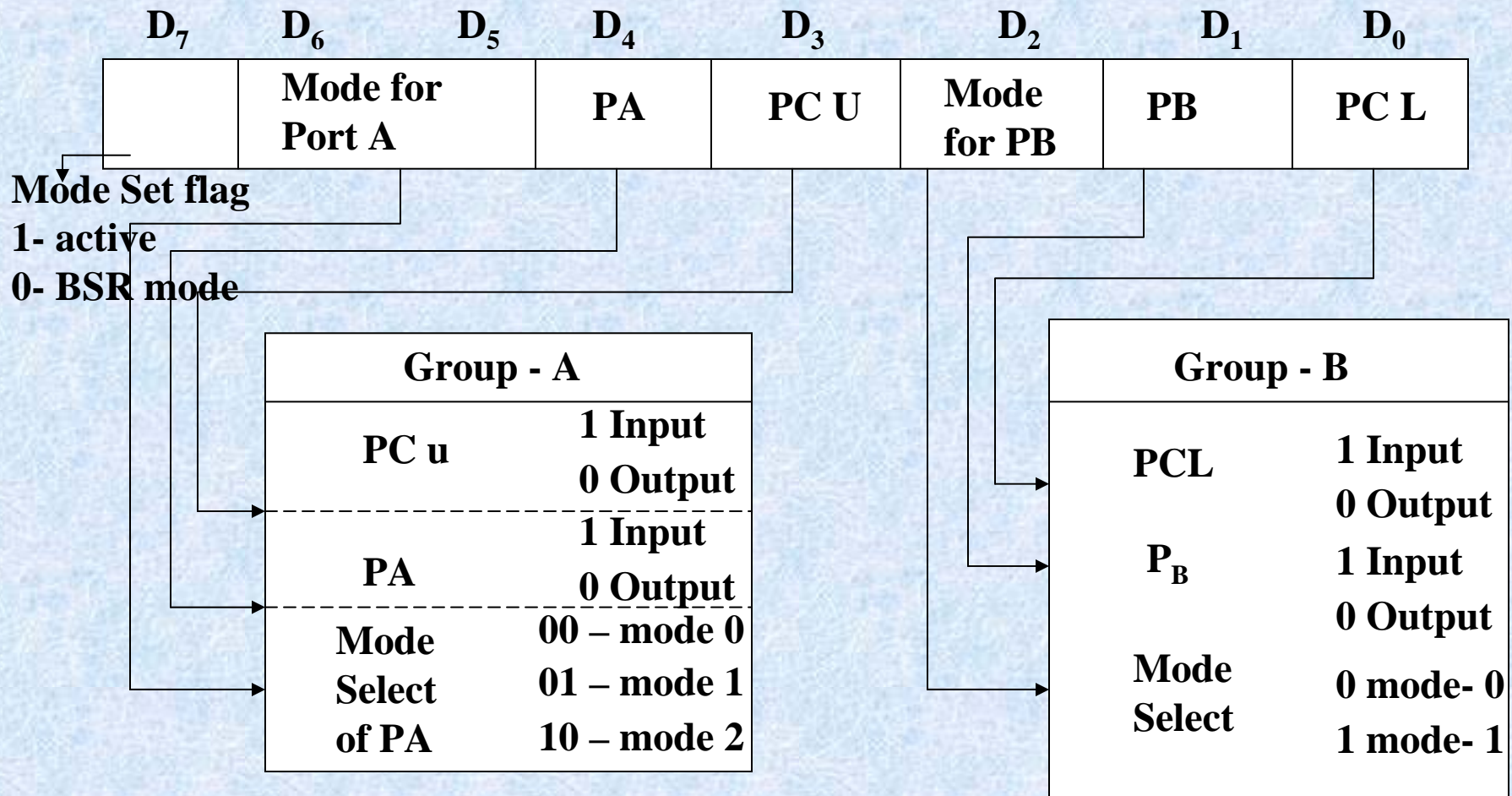
8255A Pin Configuration



Signals of 8255



Block Diagram of 8255



Control Word Format of 8255

Modes of Operation of 8255 (cont..)

b) Mode 1: (*Strobed input/output mode*) In this mode the handshaking control the input and output action of the specified port. Port C lines PC_0 - PC_2 , provide strobe or handshake lines for port B. This group which includes port B and PC_0 - PC_2 is called as group B for Strobed data input/output. Port C lines PC_3 - PC_5 provide strobe lines for port A. This group including port A and PC_3 - PC_5 from group A. Thus port C is utilized for generating handshake signals. The salient features of mode 1 are listed as follows:

Modes of Operation of 8255 (cont..)

1. Two groups – group A and group B are available for strobed data transfer.
2. Each group contains one 8-bit data I/O port and one 4-bit control/data port.
3. The 8-bit data port can be either used as input and output port. The inputs and outputs both are latched.
4. Out of 8-bit port C, PC_0 - PC_2 are used to generate control signals for port B and PC_3 - PC_5 are used to generate control signals for port A. the lines PC_6 , PC_7 may be used as independent data lines.

Modes of Operation of 8255 (cont..)

- The control signals for both the groups in input and output modes are explained as follows:

Input control signal definitions (mode 1):

- **$\overline{\text{STB}}$** (Strobe input) – If this line falls to logic low level, the data available at 8-bit input port is loaded into input latches.
- **IBF** (Input buffer full) – If this signal rises to logic 1, it indicates that data has been loaded into latches, i.e. it works as an acknowledgement. IBF is set by a low on $\overline{\text{STB}}$ and is reset by the rising edge of $\overline{\text{RD}}$ input.

Modes of Operation of 8255 (cont..)

- **INTR** (Interrupt request) – This active high output signal can be used to interrupt the CPU whenever an input device requests the service. INTR is set by a high STB pin and a high at IBF pin. INTE is an internal flag that can be controlled by the bit set/reset mode of either $PC_4(INTE_A)$ or $PC_2(INTE_B)$ as shown in fig.
- INTR is reset by a falling edge of RD input. Thus an external input device can be request the service of the processor by putting the data on the bus and sending the strobe signal.

Modes of Operation of 8255 (cont..)

Output control signal definitions (mode 1) :

- **OBF** (Output buffer full) – This status signal, whenever falls to low, indicates that CPU has written data to the specified output port. The OBF flip-flop will be set by a rising edge of WR signal and reset by a low going edge at the ACK input.
- **ACK** (Acknowledge input) – $\overline{\text{ACK}}$ signal acts as an acknowledgement to be given by an output device. $\overline{\text{ACK}}$ signal, whenever low, informs the CPU that the data transferred by the CPU to the output device through the port is received by the output device.

Modes of Operation of 8255 (cont..)

- **INTR** (Interrupt request) – Thus an output signal that can be used to interrupt the CPU when an output device acknowledges the data received from the CPU. INTR is set when ACK, OBF and INTE are 1. It is reset by a falling edge on WR input. The INTEA and INTEB flags are controlled by the bit set-reset mode of PC₆ and PC₂ respectively.

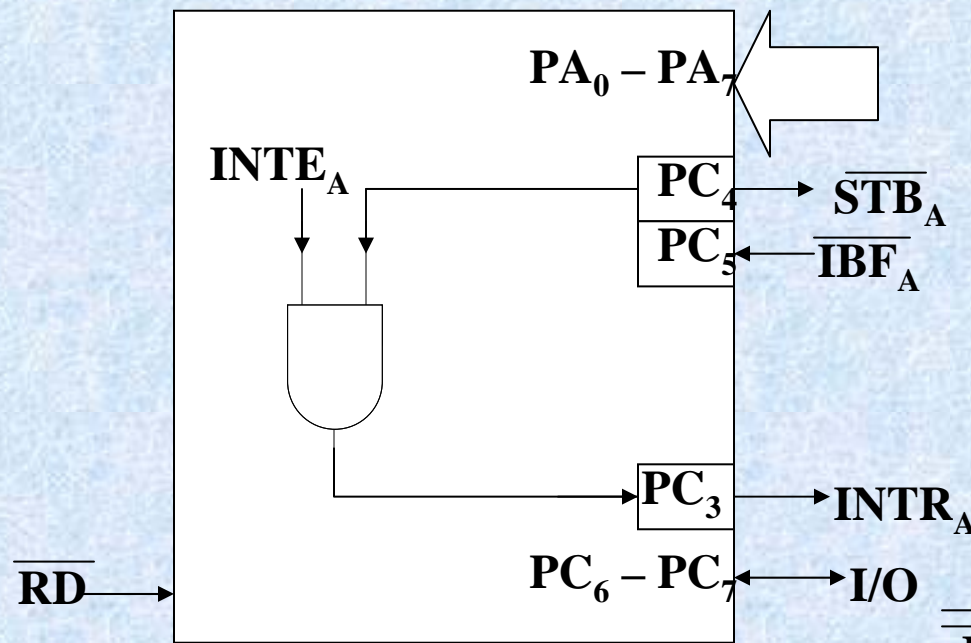
Input control signal definitions in

Mode 1

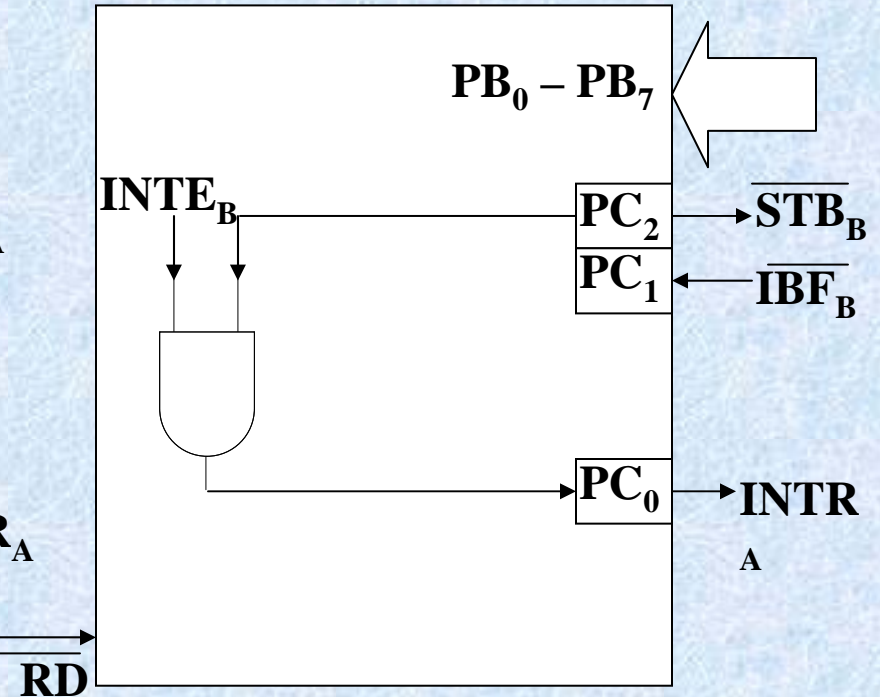
1	0	1	0	1/0	X	X	X
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀

1	X	X	X	X	1	1	X
D ₇	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀

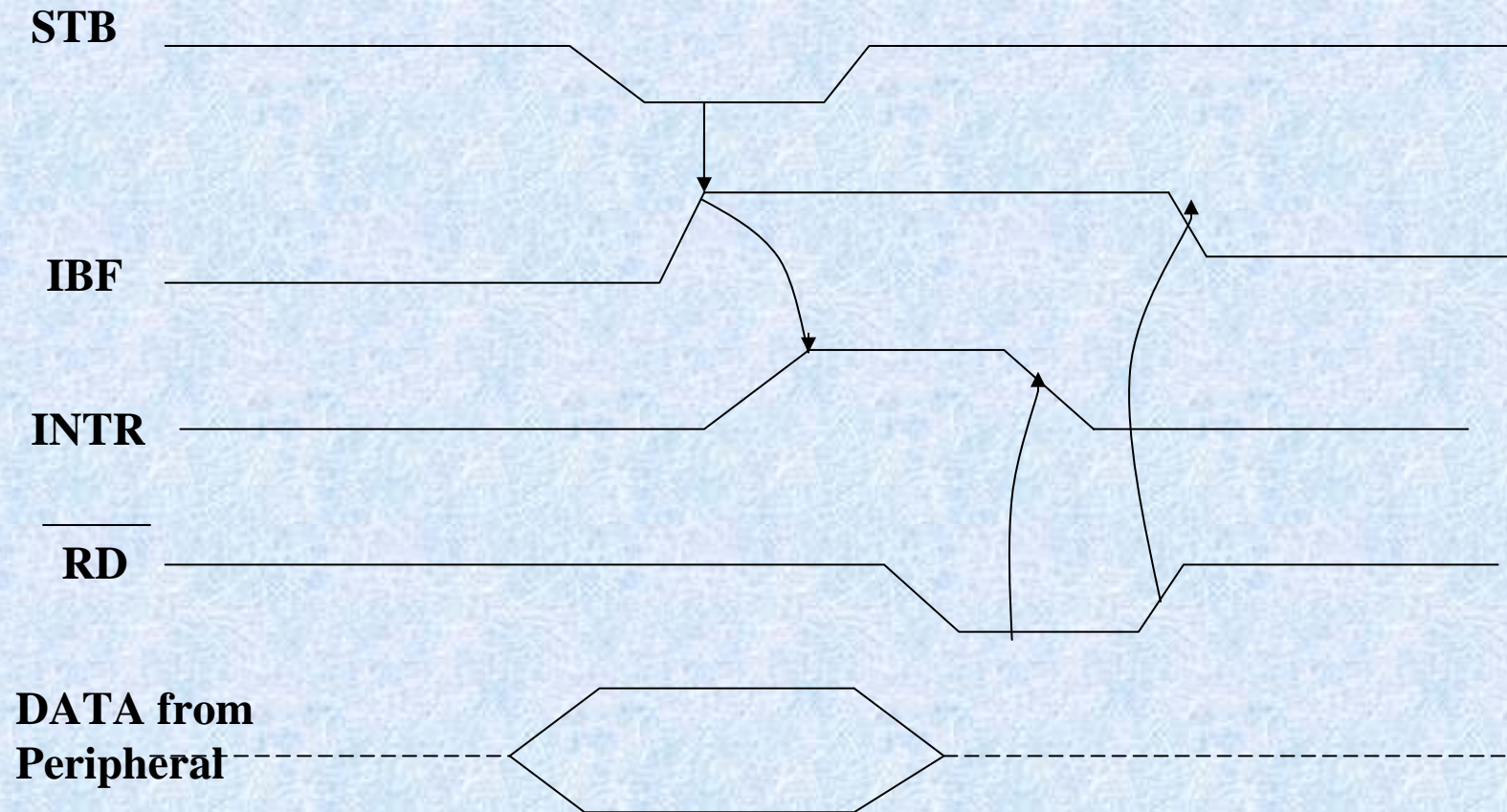
1 - Input
 0 - Output
 For PC₆ - PC₇



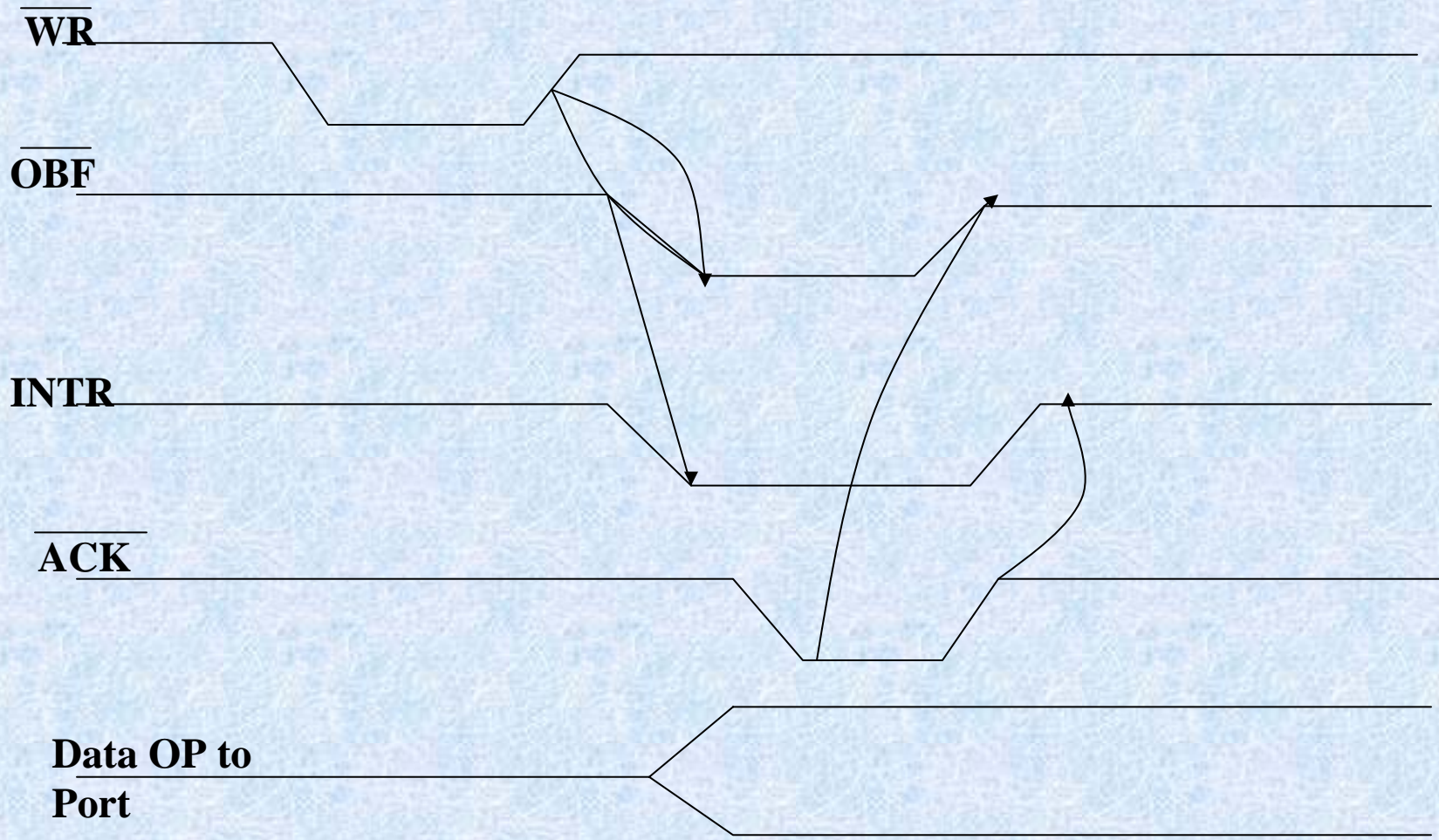
Mode 1 Control Word Group A
I/P



Mode 1 Control Word Group B
I/P



Mode 1 Strobed Input Data Transfer



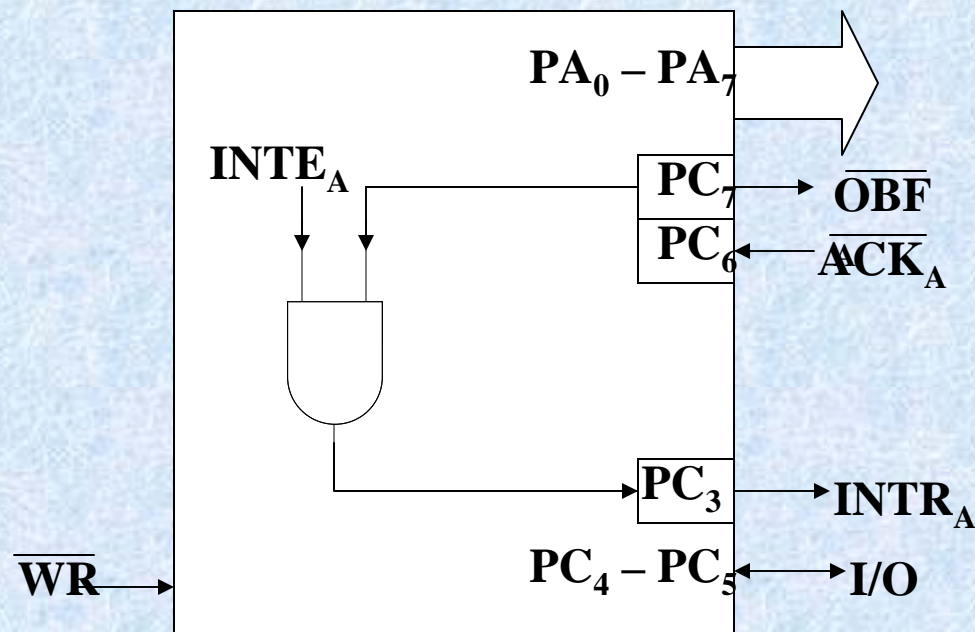
Mode 1 Strobed Data Output

Output control signal definitions Mode 1

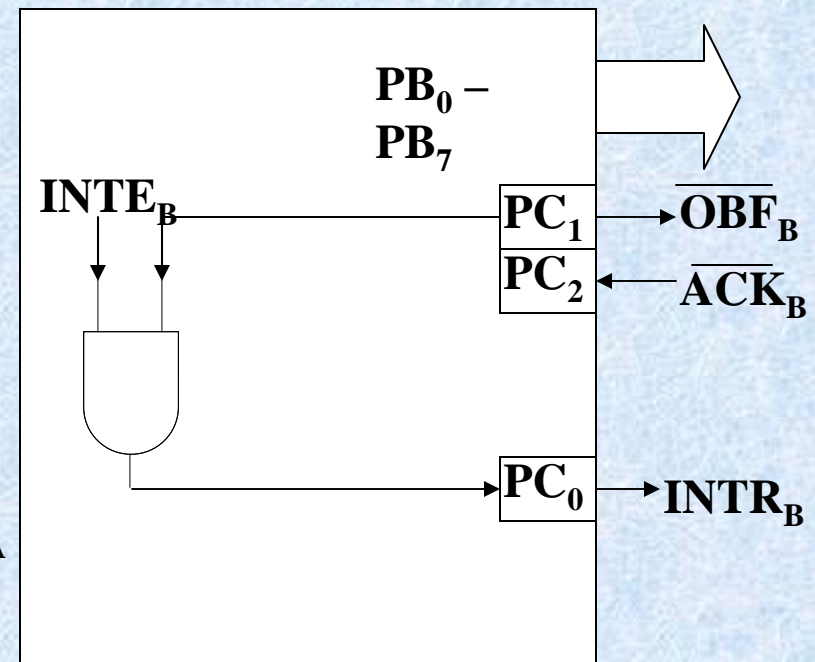
1	0	1	0	1/0	X	X	X
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

1	X	X	X	X	1	0	X
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

1 - Input
 0 - Output
 For $PC_4 - PC_5$



Mode 1 Control Word Group A



Mode 1 Control Word Group B

Modes of Operation of 8255 (cont..)

- **Mode 2 (*Strobed bidirectional I/O*):** This mode of operation of 8255 is also called as strobed bidirectional I/O. This mode of operation provides 8255 with an additional features for communicating with a peripheral device on an 8-bit data bus. Handshaking signals are provided to maintain proper data flow and synchronization between the data transmitter and receiver. The interrupt generation and other functions are similar to mode 1.
- In this mode, 8255 is a bidirectional 8-bit port with handshake signals. The RD and WR signals decide whether the 8255 is going to operate as an input port or output port.

Modes of Operation of 8255 (cont..)

- The Salient features of Mode 2 of 8255 are listed as follows:
 1. The single 8-bit port in group A is available.
 2. The 8-bit port is bidirectional and additionally a 5-bit control port is available.
 3. Three I/O lines are available at port C.($PC_2 - PC_0$)
 4. Inputs and outputs are both latched.
 5. The 5-bit control port C (PC_3-PC_7) is used for generating / accepting handshake signals for the 8-bit data transfer on port A.

Modes of Operation of 8255 (cont..)

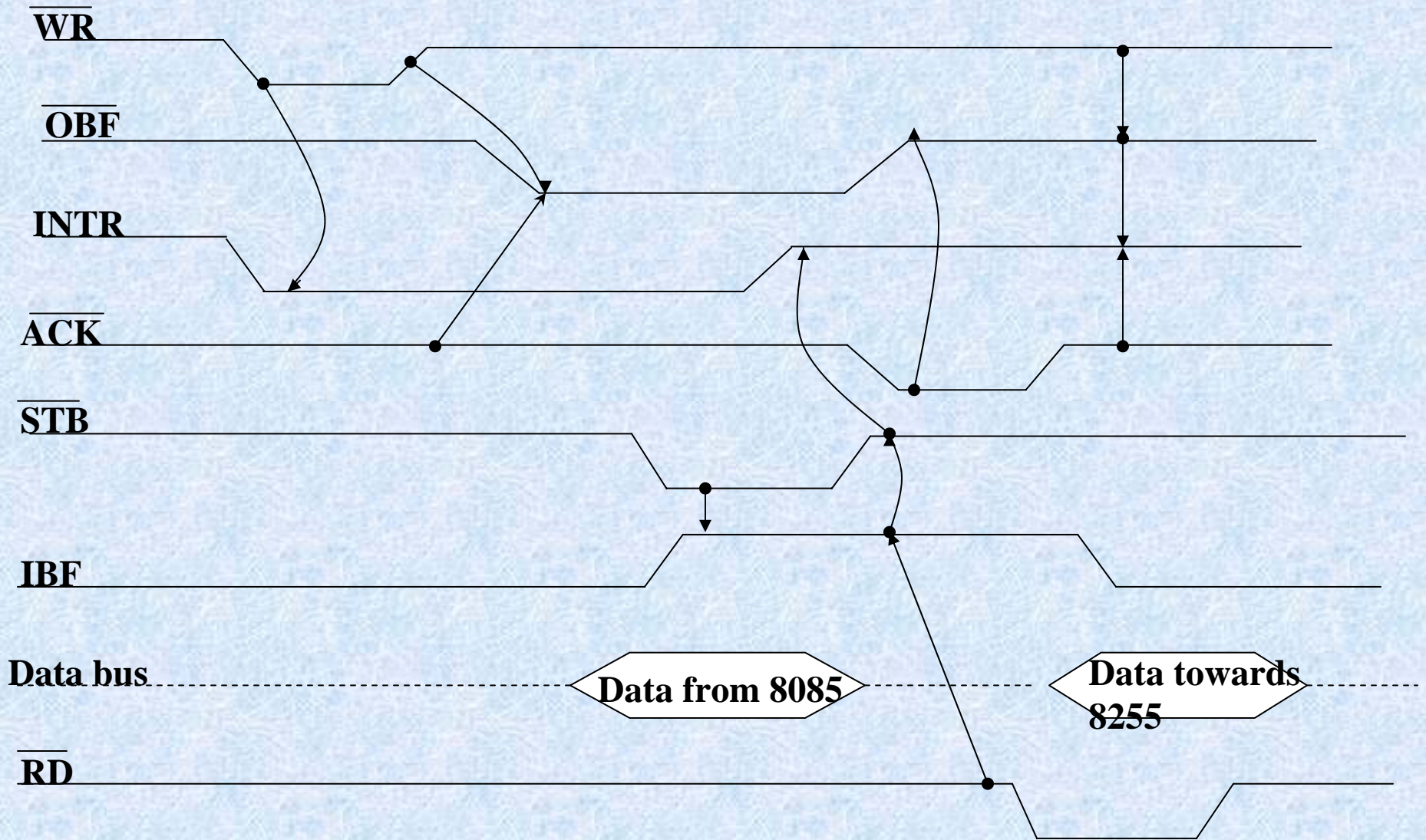
- *Control signal definitions in mode 2:*
- **INTR** – (Interrupt request) As in mode 1, this control signal is active high and is used to interrupt the microprocessor to ask for transfer of the next data byte to/from it. This signal is used for input (read) as well as output (write) operations.
- *Control Signals for Output operations:*
- **$\overline{\text{OBF}}$** (Output buffer full) – This signal, when falls to low level, indicates that the CPU has written data to port A.

Modes of Operation of 8255 (cont..)

- $\overline{\text{ACK}}$ (Acknowledge) This control input, when falls to logic low level, acknowledges that the previous data byte is received by the destination and next byte may be sent by the processor. This signal enables the internal tristate buffers to send the next data byte on port A.
- **INTE1** (A flag associated with $\overline{\text{OBF}}$) This can be controlled by bit set/reset mode with PC_6 .
- *Control signals for input operations :*
- $\overline{\text{STB}}$ (Strobe input) A low on this line is used to strobe in the data into the input latches of 8255.

Modes of Operation of 8255 (cont..)

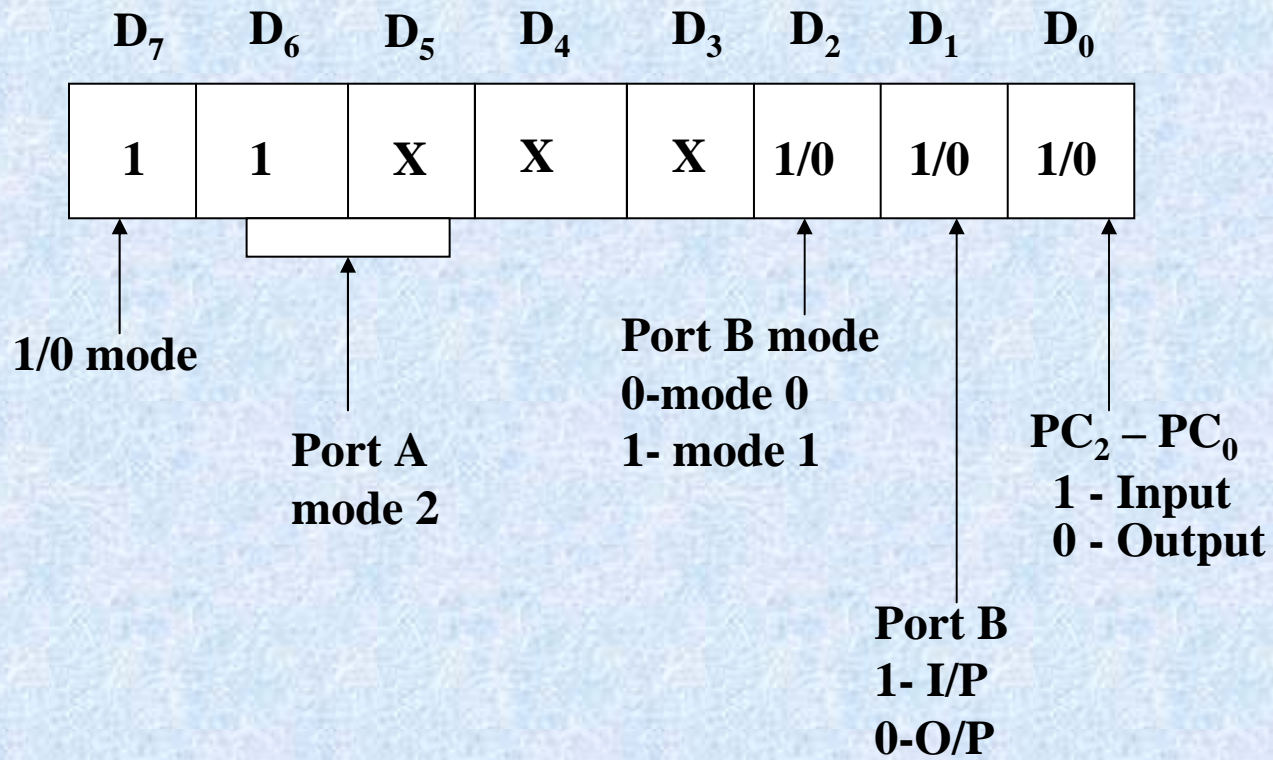
- **IBF** (Input buffer full) When the data is loaded into input buffer, this signal rises to logic '1'. This can be used as an acknowledge that the data has been received by the receiver.
- The waveforms in fig show the operation in Mode 2 for output as well as input port.
- Note: \overline{WR} must occur before \overline{ACK} and \overline{STB} must be activated before \overline{RD} .



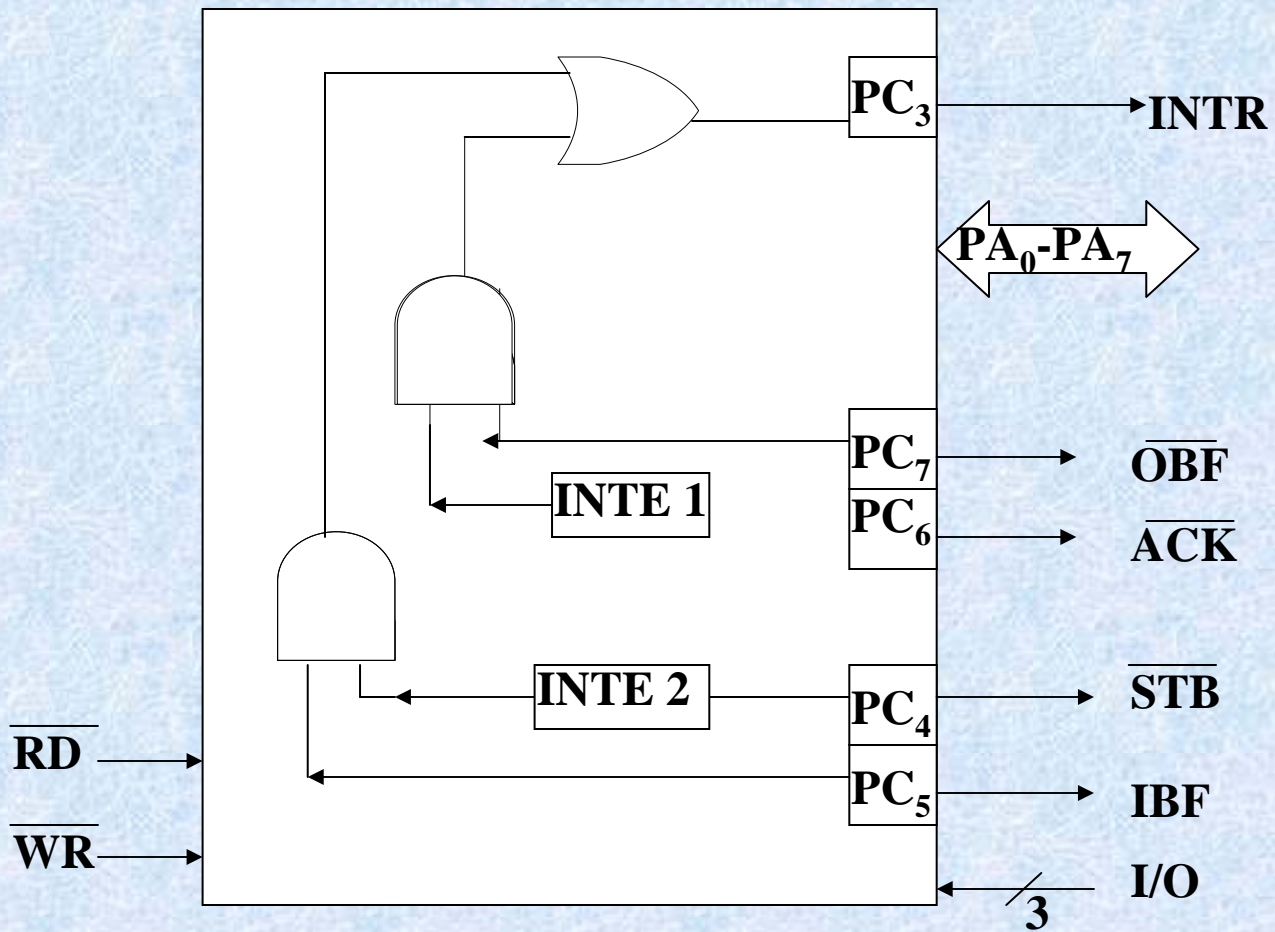
Mode 2 Bidirectional Data Transfer

Modes of Operation of 8255 (cont..)

- The following fig shows a schematic diagram containing an 8-bit bidirectional port, 5-bit control port and the relation of INTR with the control pins. Port B can either be set to Mode 0 or 1 with port A(Group A) is in Mode 2.
- Mode 2 is not available for port B. The following fig shows the control word.
- The INTR goes high only if either IBF, INTE2, STB and RD go high or OBF, INTE1, ACK and WR go high. The port C can be read to know the status of the peripheral device, in terms of the control signals, using the normal I/O instructions.



Mode 2 control word



Mode 2 pins