8086 Microprocessor (cont..)

- It is a 16 bit µp.
- 8086 has a 20 bit address bus can access upto 2^{20} memory locations (1 MB) .
- It can support upto 64K I/O ports.
- It provides 14, 16-bit registers.
- It has multiplexed address and data bus AD_0- AD_{15} and A_{16} – A_{19}.

8086 Microprocessor (cont..)

- It requires single phase clock with 33% duty cycle to provide internal timing.
- 8086 is designed to operate in two modes, Minimum and Maximum.
- It can prefetches upto 6 instruction bytes from memory and queues them in order to speed up instruction execution.
- It requires +5V power supply.
- A 40 pin dual in line package.

8086 Microprocessor (cont..)

Minimum and Maximum Modes:

- The minimum mode is selected by applying logic 1 to the MN / MX# input pin. This is a single microprocessor configuration.
- The maximum mode is selected by applying logic 0 to the MN / MX# input pin. This is a multi micro processors configuration.

8086 Microprocessor (cont..)

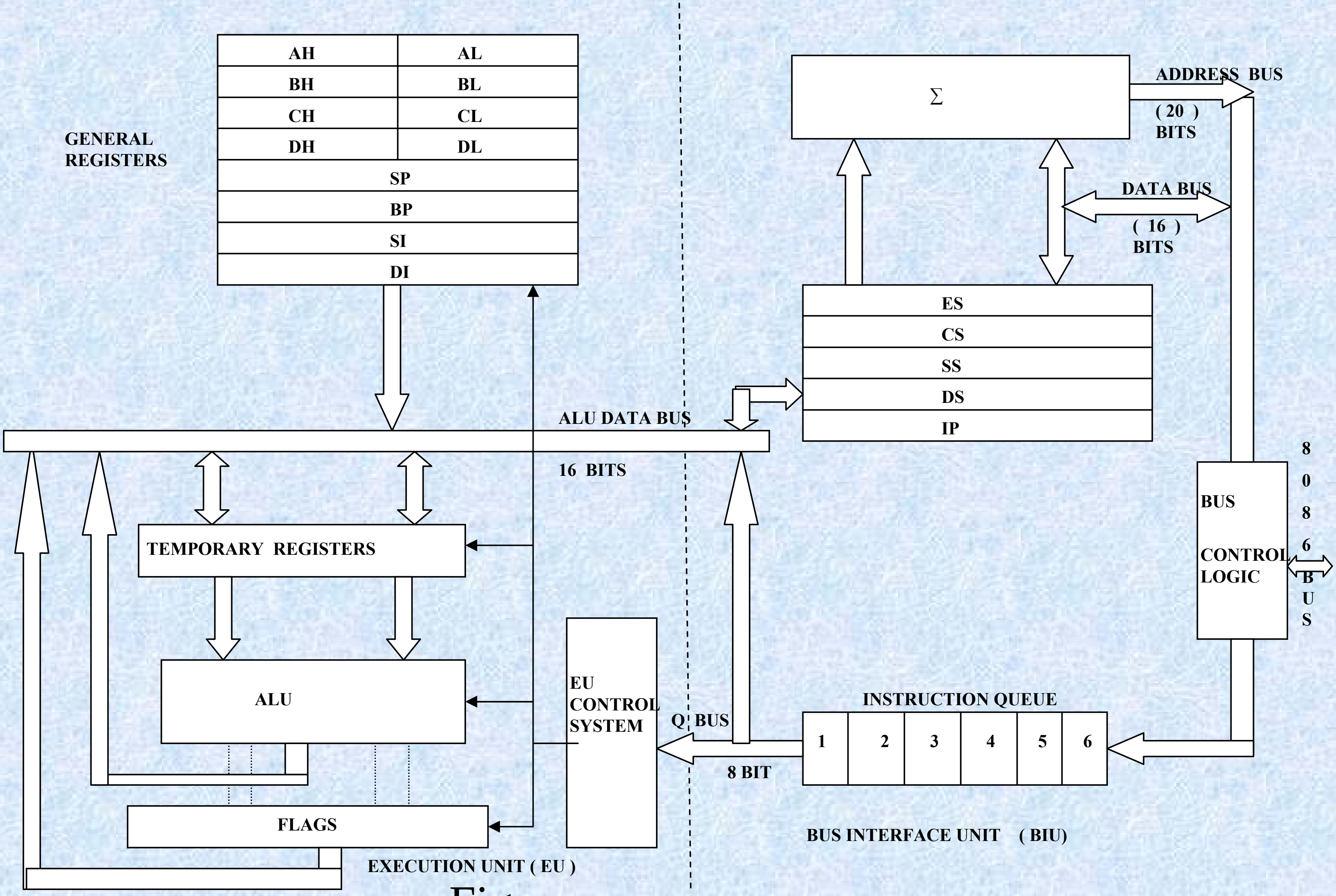
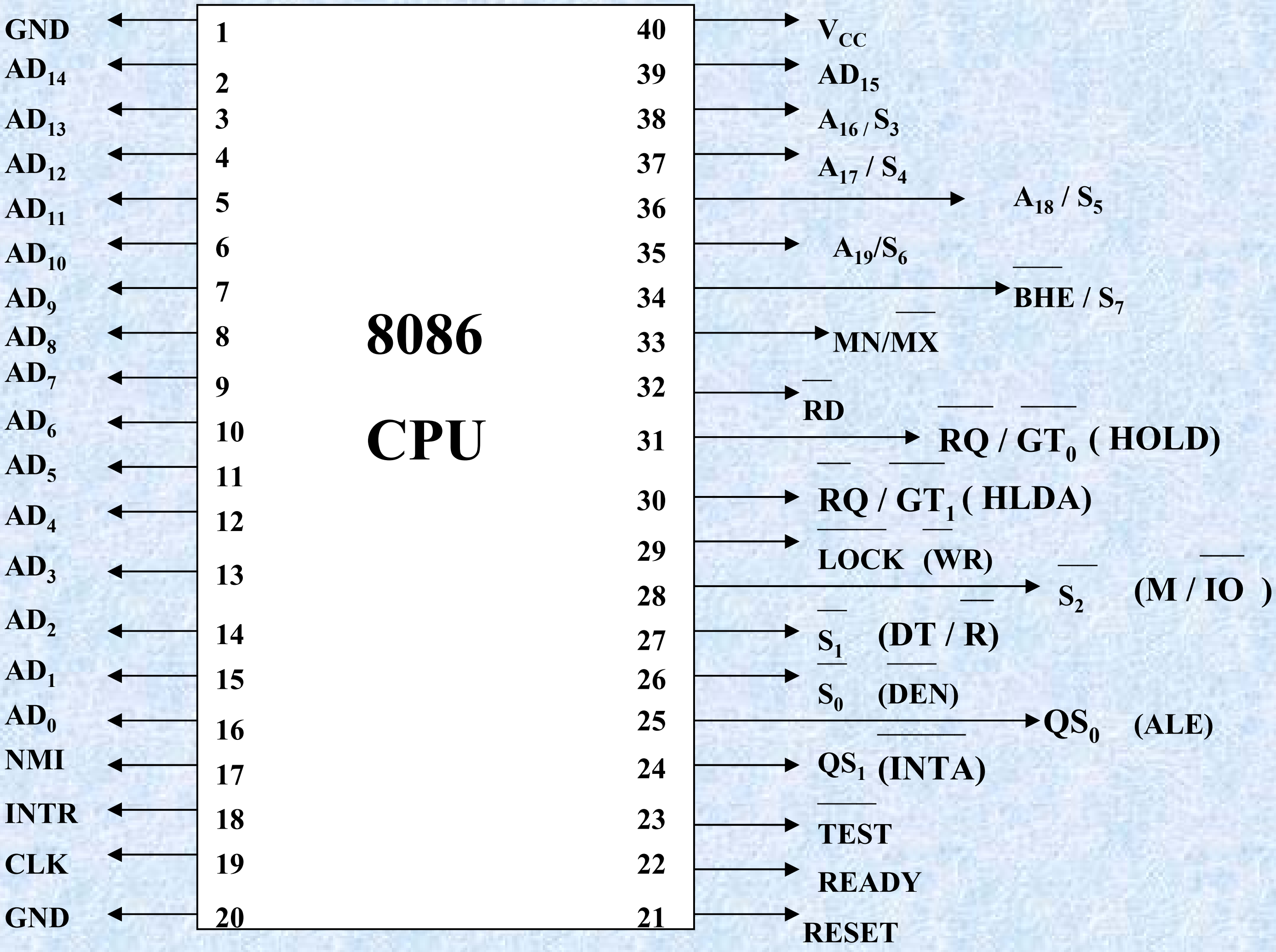
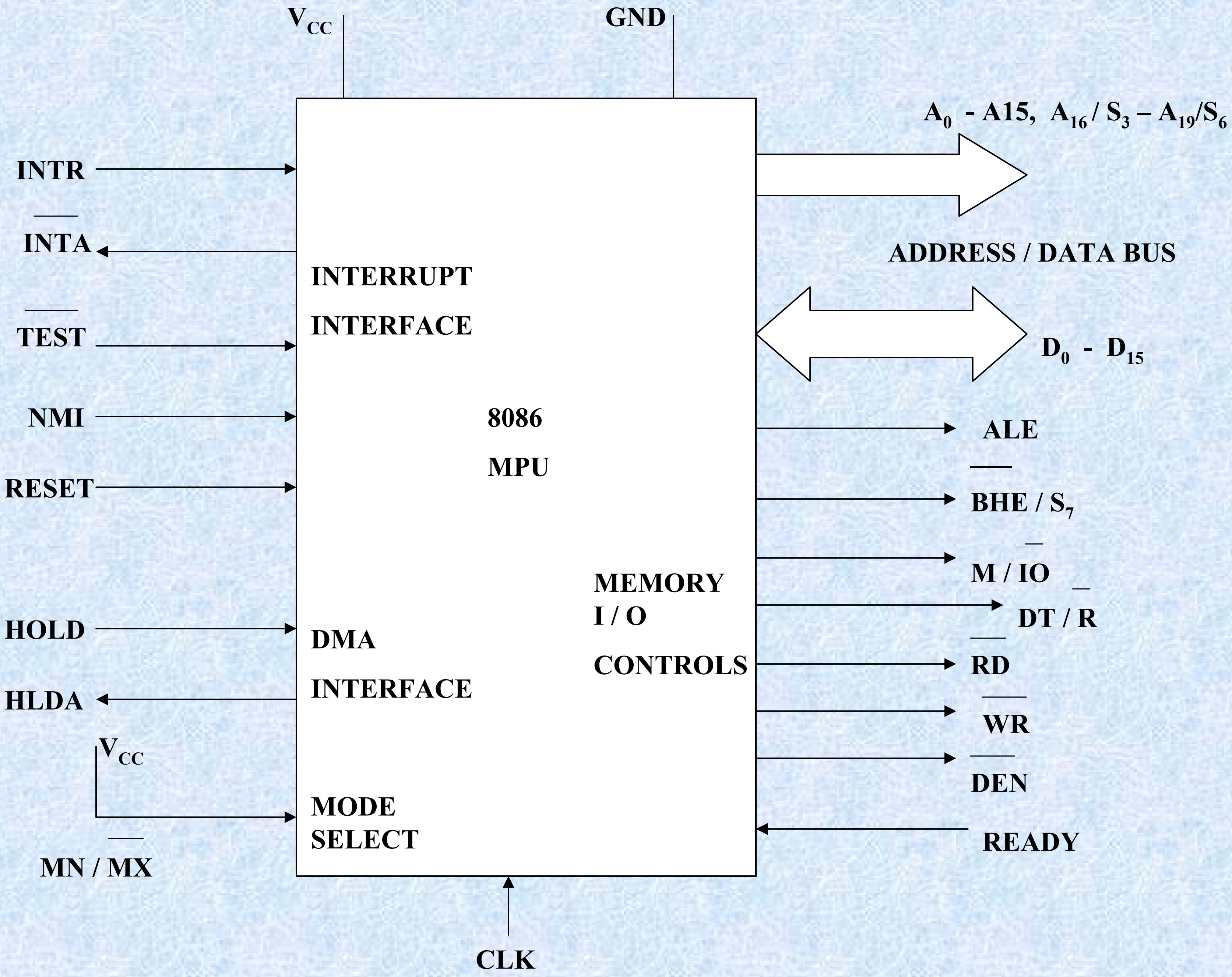


Fig:

Pin Diagram of 8086



GND	1	40	V_{CC}
AD_{14}	2	39	AD_{15}
AD_{13}	3	38	A_{16} / S_3
AD_{12}	4	37	A_{17} / S_4
AD_{11}	5	36	A_{18} / S_5
AD_{10}	6	35	A_{19}/S_6
AD_9	7	34	$\overline{BHE}$ / S_7
AD_8	8	33	MN/$\overline{MX}$
AD_7	9	32	$\overline{RD}$
AD_6	10	31	$\overline{RQ}$ / $\overline{GT_0}$ (HOLD)
AD_5	11	30	$\overline{RQ}$ / $\overline{GT_1}$ (HLDA)
AD_4	12	29	$\overline{LOCK}$ ($\overline{WR}$)
AD_3	13	28	$\overline{S_2}$ (M / $\overline{IO}$)
AD_2	14	27	$\overline{S_1}$ (DT / $\overline{R}$)
AD_1	15	26	$\overline{S_0}$ ($\overline{DEN}$)
AD_0	16	25	QS_0 (ALE)
NMI	17	24	QS_1 ($\overline{INTA}$)
INTR	18	23	$\overline{TEST}$
CLK	19	22	READY
GND	20	21	RESET



V_{CC}

GND

A_0 - A15, $A_{16}/S_3 – A_{19}/S_6$

ADDRESS / DATA BUS

D_0 - D_{15}

INTR

$\overline{\text{INTA}}$

$\overline{\text{TEST}}$

NMI

RESET

HOLD

HLDA

V_{CC}

MN / $\overline{\text{MX}}$

INTERRUPT INTERFACE

8086 MPU

DMA INTERFACE

MODE SELECT

MEMORY I / O CONTROLS

ALE

$\overline{\text{BHE}}$ / S_7

M / $\overline{\text{IO}}$

DT / $\overline{\text{R}}$

$\overline{\text{RD}}$

$\overline{\text{WR}}$

$\overline{\text{DEN}}$

READY

CLK

Internal Architecture of 8086

- 8086 has two blocks BIU and EU.
- The BIU performs all bus operations such as instruction fetching, reading and writing operands for memory and calculating the addresses of the memory operands.
- The instruction bytes are transferred to the instruction queue.
- EU executes instructions from the instruction system byte queue.

Internal Architecture of 8086 (cont..)

- Both units operate asynchronously to give the 8086 an overlapping instruction fetch and execution mechanism which is called as Pipelining. This results in efficient use of the system bus and system performance.
- BIU contains Instruction queue, Segment registers, Instruction pointer, Address adder.
- EU contains Control circuitry, Instruction decoder, ALU, Pointer and Index register, Flag register.

Internal Architecture of 8086 (cont..)

- Bus Interfacr Unit**:**
- It provides a full 16 bit bidirectional data bus and 20 bit address bus.
- The bus interface unit is responsible for performing all external bus operations.

Specifically it has the following functions:

- Instruction fetch, Instruction queuing, Operand fetch and storage, Address relocation and Bus control.
- The BIU uses a mechanism known as an instruction stream queue to implement a ***pipeline architecture.***

Internal Architecture of 8086 (cont..)

- This queue permits prefetch of up to six bytes of instruction code. When ever the queue of the BIU is not full, it has room for at least two more bytes and at the same time the EU is not requesting it to read or write operands from memory, the BIU is free to look ahead in the program by prefetching the next sequential instruction.
- These prefetching instructions are held in its FIFO queue. With its 16 bit data bus, the BIU fetches two instruction bytes in a single memory cycle.
- After a byte is loaded at the input end of the queue, it automatically shifts up through the FIFO to the empty location nearest the output.

Internal Architecture of 8086 (cont..)

- The EU accesses the queue from the output end. It reads one instruction byte after the other from the output of the queue. If the queue is full and the EU is not requesting access to operand in memory.
- These intervals of no bus activity, which may occur between bus cycles are known as ***Idle state***.
- If the BIU is already in the process of fetching an instruction when the EU request it to read or write operands from memory or I/O, the BIU first completes the instruction fetch bus cycle before initiating the operand read / write cycle.

Internal Architecture of 8086 (cont..)

- The BIU also contains a dedicated adder which is used to generate the 20 bit physical address that is output on the address bus. This address is formed by adding an appended 16 bit segment address and a 16 bit offset address.
- For example, the physical address of the next instruction to be fetched is formed by combining the current contents of the code segment CS register and the current contents of the instruction pointer IP register.
- The BIU is also responsible for generating bus control signals such as those for memory read or write and I/O read or write.

Internal Architecture of 8086 (cont..)

- **EXECUTION UNIT** : The Execution unit is responsible for decoding and executing all instructions.
- The EU extracts instructions from the top of the queue in the BIU, decodes them, generates operands if necessary, passes them to the BIU and requests it to perform the read or write bys cycles to memory or I/O and perform the operation specified by the instruction on the operands.
- During the execution of the instruction, the EU tests the status and control flags and updates them based on the results of executing the instruction.

Internal Architecture of 8086 (cont..)

- If the queue is empty, the EU waits for the next instruction byte to be fetched and shifted to top of the queue.
- When the EU executes a branch or jump instruction, it transfers control to a location corresponding to another set of sequential instructions.
- Whenever this happens, the BIU automatically resets the queue and then begins to fetch instructions from this new location to refill the queue.

Internal Architecture of 8086 (cont..)

COMMON SIGNALS		
Name	**Function**	**Type**
$AD_{15} - AD_{0}$	Address/ Data Bus	Bidirectional 3 - state
$A_{19} / S_{6} - A_{16} / S_{3}$	Address / Status	Output 3 - State
$\overline{BHE}$ / S 7	Bus High Enable / Status	Output 3- State
MN / $\overline{MX}$	Minimum / Maximum Mode Control	Input
$\overline{RD}$	Read Control	Output 3- State
TEST	Wait On Test Control	Input
READY	Wait State Controls	Input
RESET	System Reset	Input
NMI	Non - Maskable Interrupt Request	Input
INTR	Interrupt Request	Input
CLK	System Clock	Input
Vcc	+ 5 V	Input
GND	Ground	

Internal Architecture of 8086 (cont..)

Minimum Mode Signals ($MN/\overline{MX}$ = Vcc)

Name	Function	Type
HOLD	Hold Request	Input
HLDA	Hold Acknowledge	Output
$\overline{WR}$	Write Control	Output, 3- state
$M/\overline{IO}$	Memory or IO Control	Output, 3-State
$DT/\overline{R}$	Data Transmit / Receiver	Output, 3- State
$\overline{DEN}$	Date Enable	Output, 3-State
ALE	Address Latch Enable	Output
$\overline{INTA}$	Interrupt Acknowledge	Output

Internal Architecture of 8086 (cont..)

Maximum mode signals (MN / $M\overline{X}$ = GND)

Name	Function	Type
RQ / $\overline{\text{GT1, 0}}$	**Request / Grant Bus Access Control**	**Bidirectional**
$\overline{\text{LOCK}}$	**Bus Priority Lock Control**	**Output, 3- State**
$\overline{S}_2 – \overline{S}_0$	**Bus Cycle Status**	**Output, 3- State**
QS1, QS0	**Instruction Queue Status**	**Output**

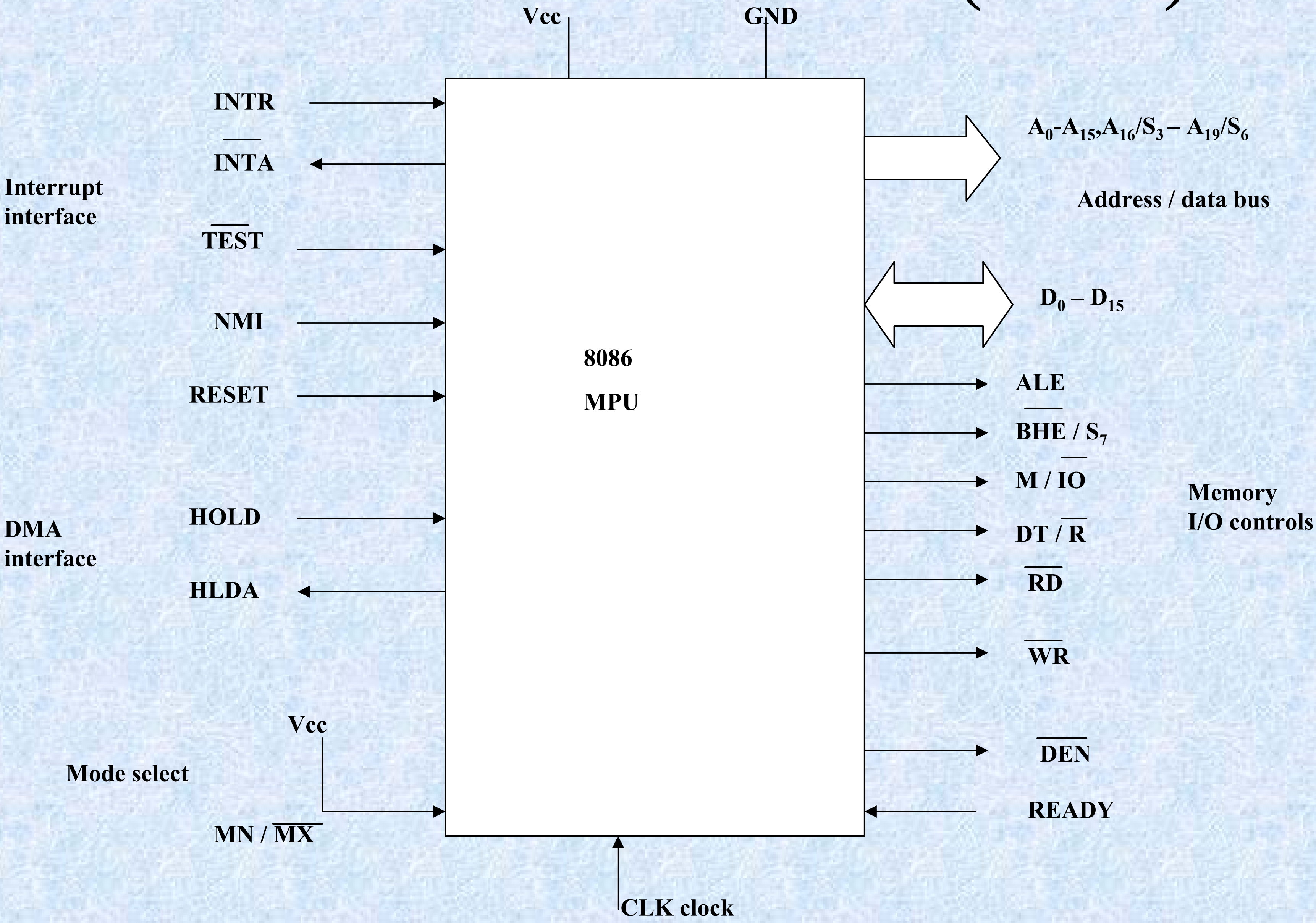
Minimum Mode Interface

- When the Minimum mode operation is selected, the 8086 provides all control signals needed to implement the memory and I/O interface.
- The minimum mode signal can be divided into the following basic groups : address/data bus, status, control, interrupt and DMA.
- **Address/Data Bus** : these lines serve two functions. As an address bus is 20 bits long and consists of signal lines A_0 through A_{19}. A_{19} represents the MSB and A_0 LSB. A 20bit address gives the 8086 a 1Mbyte memory address space. More over it has an independent I/O address space which is 64K bytes in length.

Minimum Mode Interface (cont..)

- The 16 data bus lines D_0 through D_{15} are actually multiplexed with address lines A_0 through A_{15} respectively. By multiplexed we mean that the bus work as an address bus during first machine cycle and as a data bus during next machine cycles. D_{15} is the MSB and D_0 LSB.
- When acting as a data bus, they carry read/write data for memory, input/output data for I/O devices, and interrupt type codes from an interrupt controller.

Minimum Mode Interface (cont..)



Block Diagram of the Minimum Mode 8086 MPU

Minimum Mode Interface (cont..)

- **Status signal** : The four most significant address lines A_{19} through A_{16} are also multiplexed but in this case with status signals S_6 through S_3. These status bits are output on the bus at the same time that data are transferred over the other bus lines.
- Bit S_4 and S_3 together from a 2 bit binary code that identifies which of the 8086 internal segment registers are used to generate the physical address that was output on the address bus during the current bus cycle.
- Code S_4S_3 = 00 identifies a register known as ***extra segment register*** as the source of the segment address.

Minimum Mode Interface (cont..)

S_4	S_3	Segment Register
0	0	Extra
0	1	Stack
1	0	Code / none
1	1	Data

Memory segment status codes.

Minimum Mode Interface (cont..)

- Status line S_5 reflects the status of another internal characteristic of the 8086. It is the logic level of the internal enable flag. The last status bit S_6 is always at the logic 0 level.
- **Control Signals** : The control signals are provided to support the 8086 memory I/O interfaces. They control functions such as when the bus is to carry a valid address in which direction data are to be transferred over the bus, when valid write data are on the bus and when to put read data on the system bus.

Minimum Mode Interface (cont..)

- ALE is a pulse to logic 1 that signals external circuitry when a valid address word is on the bus. This address must be latched in external circuitry on the 1-to-0 edge of the pulse at ALE.
- Another control signal that is produced during the bus cycle is BHE bank high enable. Logic 0 on this used as a memory enable signal for the most significant byte half of the data bus D_8 through D_1. These lines also serves a second function, which is as the S_7 status line.
- Using the M/IO and DT/R lines, the 8086 signals which type of bus cycle is in progress and in which direction data are to be transferred over the bus.

Minimum Mode Interface (cont..)

- The logic level of $\overline{M}$/IO tells external circuitry whether a memory or I/O transfer is taking place over the bus. Logic 1 at this output signals a memory operation and logic 0 an I/O operation.
- The direction of data transfer over the bus is signaled by the logic level output at DT/$\overline{R}$. When this line is logic 1 during the data transfer part of a bus cycle, the bus is in the transmit mode. Therefore, data are either written into memory or output to an I/O device.
- On the other hand, logic 0 at DT/$\overline{R}$ signals that the bus is in the receive mode. This corresponds to reading data from memory or input of data from an input port.

Minimum Mode Interface (cont..)

- The signal read $\overline{RD}$ and write $\overline{WR}$ indicates that a read bus cycle or a write bus cycle is in progress. The 8086 switches $\overline{WR}$ to logic 0 to signal external device that valid write or output data are on the bus.
- On the other hand, $\overline{RD}$ indicates that the 8086 is performing a read of data of the bus. During read operations, one other control signal is also supplied. This is $\overline{DEN}$ (data enable) and it signals external devices when they should put data on the bus.
- There is one other control signal that is involved with the memory and I/O interface. This is the READY signal.

Minimum Mode Interface (cont..)

- READY signal is used to insert wait states into the bus cycle such that it is extended by a number of clock periods. This signal is provided by an external clock generator device and can be supplied by the memory or I/O sub-system to signal the 8086 when they are ready to permit the data transfer to be completed.
- **Interrupt signals** : The key interrupt interface signals are interrupt request (INTR) and interrupt acknowledge ($\overline{\text{INTA}}$).
- INTR is an input to the 8086 that can be used by an external device to signal that it need to be serviced.

Minimum Mode Interface (cont..)

- Logic 1 at INTR represents an active interrupt request. When an interrupt request has been recognized by the 8086, it indicates this fact to external circuit with pulse to logic 0 at the $\overline{\text{INTA}}$ output.
- The $\overline{\text{TEST}}$ input is also related to the external interrupt interface. Execution of a WAIT instruction causes the 8086 to check the logic level at the $\overline{\text{TEST}}$ input.
- If the logic 1 is found, the MPU suspend operation and goes into the idle state. The 8086 no longer executes instructions, instead it repeatedly checks the logic level of the $\overline{\text{TEST}}$ input waiting for its transition back to logic 0.

Minimum Mode Interface (cont..)

- As $\overline{\text{TEST}}$ switches to 0, execution resume with the next instruction in the program. This feature can be used to synchronize the operation of the 8086 to an event in external hardware.
- There are two more inputs in the interrupt interface: the nonmaskable interrupt NMI and the reset interrupt RESET.
- On the 0-to-1 transition of NMI control is passed to a nonmaskable interrupt service routine. The RESET input is used to provide a hardware reset for the 8086. Switching RESET to logic 0 initializes the internal register of the 8086 and initiates a reset service routine.

Minimum Mode Interface.

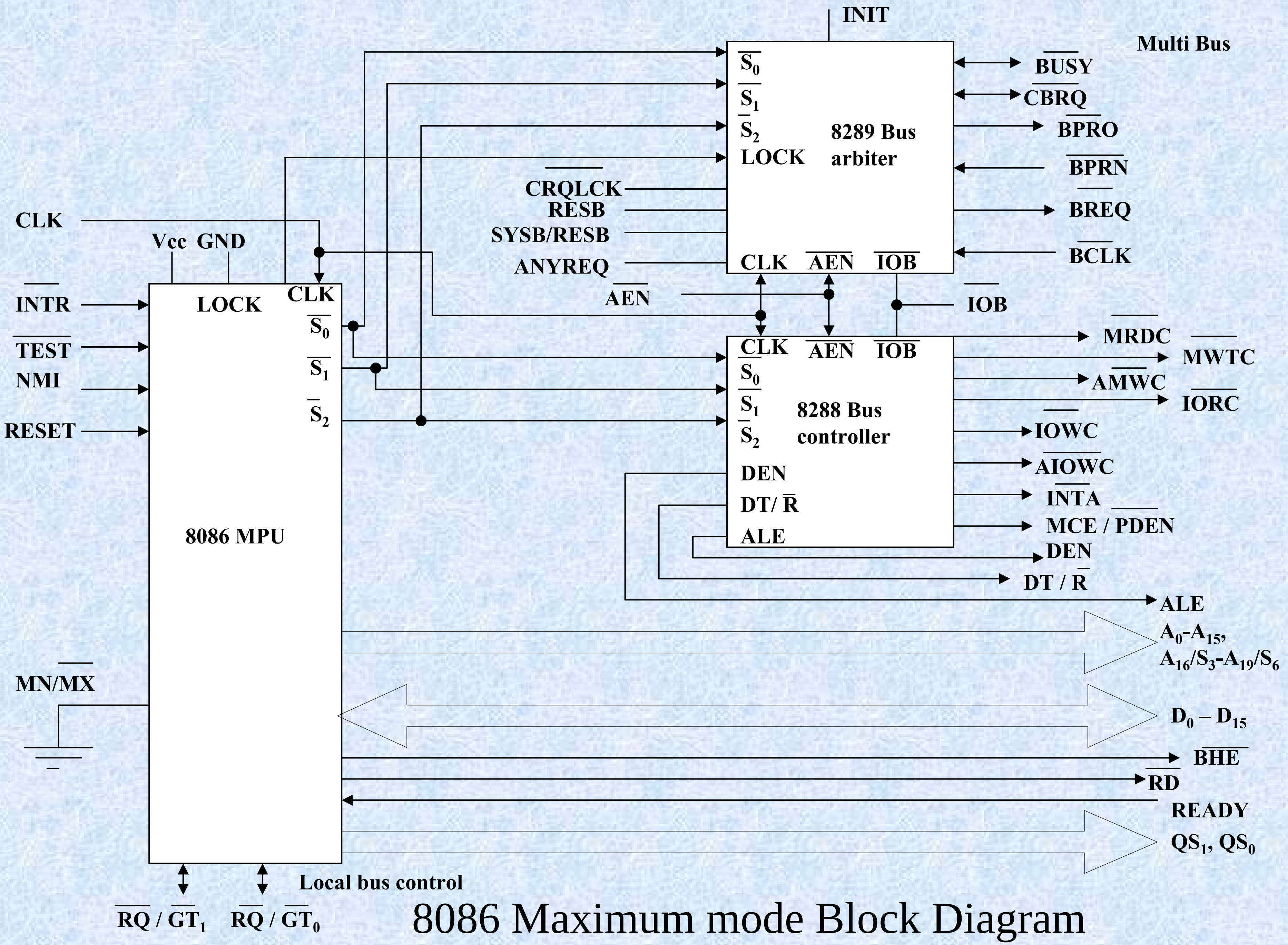
- **DMA Interface signals** :The direct memory access DMA interface of the 8086 minimum mode consist of the HOLD and HLDA signals.
- When an external device wants to take control of the system bus, it signals to the 8086 by switching HOLD to the logic 1 level. At the completion of the current bus cycle, the 8086 enters the hold state. In the hold state, signal lines AD_0 through AD_{15}, A_{16}/S_3 through A_{19}/S_6, $\overline{\text{BHE}}$, $\overline{\text{M}}$/IO, DT/$\overline{\text{R}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{DEN}}$ and INTR are all in the high Z state. The 8086 signals external device that it is in this state by switching its HLDA output to logic 1 level.

Maximum Mode Interface

- When the 8086 is set for the maximum-mode configuration, it provides signals for implementing a multiprocessor / coprocessor system environment.
- By multiprocessor environment we mean that one microprocessor exists in the system and that each processor is executing its own program.
- Usually in this type of system environment, there are some system resources that are common to all processors.
- They are called as ***global resources***. There are also other resources that are assigned to specific processors. These are known as ***local*** or ***private resources***.

Maximum Mode Interface (cont..)

- Coprocessor also means that there is a second processor in the system. In this two processor does not access the bus at the same time.
- One passes the control of the system bus to the other and then may suspend its operation.
- In the maximum-mode 8086 system, facilities are provided for implementing allocation of global resources and passing bus control to other microprocessor or coprocessor.



8086 Maximum mode Block Diagram

Maximum Mode Interface (cont..)

- **8288 Bus Controller – Bus Command and Control Signals**: 8086 does not directly provide all the signals that are required to control the memory, I/O and interrupt interfaces.
- Specially the $\overline{WR}$, M/$\overline{IO}$, DT/$\overline{R}$, $\overline{DEN}$, $\overline{ALE}$ and $\overline{INTA}$, signals are no longer produced by the 8086. Instead it outputs three status signals $\overline{S_0}$, $\overline{S_1}$, $\overline{S_2}$ prior to the initiation of each bus cycle. This 3- bit bus status code identifies which type of bus cycle is to follow.
- $\overline{S_2}\overline{S_1}\overline{S_0}$ are input to the external bus controller device, the bus controller generates the appropriately timed command and control signals.

Maximum Mode Interface (cont..)

Status Inputs			CPU Cycles	8288 Command
$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$		
0	0	0	Interrupt Acknowledge	$\overline{\text{INTA}}$
0	0	1	Read I/O Port	$\overline{\text{IORC}}$
0	1	0	Write I/O Port	$\overline{\text{IOWC}}$, $\overline{\text{AIOWC}}$
0	1	1	Halt	None
1	0	0	Instruction Fetch	$\overline{\text{MRDC}}$
1	0	1	Read Memory	$\overline{\text{MRDC}}$
1	1	0	Write Memory	$\overline{\text{MWTC}}$, $\overline{\text{AMWC}}$
1	1	1	Passive	None

Bus Status Codes

Maximum Mode Interface (cont..)

- The 8288 produces one or two of these eight command signals for each bus cycles. For instance, when the 8086 outputs the code $\overline{S_2}\,\overline{S_1}\,\overline{S_0}$ equals 001, it indicates that an ***I/O read cycle*** is to be performed.
- In the code 111 is output by the 8086, it is signaling that no bus activity is to take place.
- The control outputs produced by the 8288 are DEN, $DT/\overline{R}$ and ALE. These 3 signals provide the same functions as those described for the minimum system mode. This set of bus commands and control signals is compatible with the Multibus and industry standard for interfacing microprocessor systems.

Maximum Mode Interface (cont..)

- **8289 Bus Arbiter – Bus Arbitration and Lock Signals** : This device permits processors to reside on the system bus. It does this by implementing the Multibus arbitration protocol in an 8086-based system.
- Addition of the 8288 bus controller and 8289 bus arbiter frees a number of the 8086 pins for use to produce control signals that are needed to support multiple processors.
- Bus priority lock ($\overline{\mathrm{LOCK}}$) is one of these signals. It is input to the bus arbiter together with status signals $\overline{S}_0$ through $\overline{S}_2$.

Maximum Mode Interface (cont..)

- ***The output of 8289 are bus arbitration signals***: *bus busy* ($\overline{\text{BUSY}}$), *common bus request* ($\overline{\text{CBRQ}}$), *bus priority out* ($\overline{\text{BPRO}}$), *bus priority in* ($\overline{\text{BPRN}}$), *bus request* ($\overline{\text{BREQ}}$) and *bus clock* ($\overline{\text{BCLK}}$).
- They correspond to the bus exchange signals of the Multibus and are used to lock other processor off the system bus during the execution of an instruction by the 8086.
- In this way the processor can be assured of uninterrupted access to common system resources such as ***global memory.***

Maximum Mode Interface (cont..)

- **Queue Status Signals** : Two new signals that are produced by the 8086 in the maximum-mode system are queue status outputs QS_0 and QS_1. Together they form a 2-bit queue status code, QS_1QS_0.
- Following table shows the four different queue status.

Maximum Mode Interface (cont..)

QS_1	QS_0	Queue Status
0 (low)	0	No Operation. During the last clock cycle, nothing was taken from the queue.
0	1	First Byte. The byte taken from the queue was the first byte of the instruction.
1 (high)	0	Queue Empty. The queue has been reinitialized as a result of the execution of a transfer instruction.
1	1	Subsequent Byte. The byte taken from the queue was a subsequent byte of the instruction.

Queue status codes

Maximum Mode Interface (cont..)

- **Local Bus Control Signal – Request / Grant Signals**: In a maximum mode configuration, the minimum mode HOLD, HLDA interface is also changed. These two are replaced by request/grant lines $\overline{RQ}/\ \overline{GT}_0$ and $\overline{RQ}/\ \overline{GT}_1$, respectively. They provide a prioritized bus access mechanism for accessing the local bus.

Minimum Mode 8086 System

- In a minimum mode 8086 system, the microprocessor 8086 is operated in minimum mode by strapping its MN/$\overline{\text{MX}}$ pin to logic 1.
- In this mode, all the control signals are given out by the microprocessor chip itself. There is a single microprocessor in the minimum mode system.
- The remaining components in the system are latches, transreceivers, clock generator, memory and I/O devices. Some type of chip selection logic may be required for selecting memory or I/O devices, depending upon the address map of the system.

Minimum Mode 8086 System (cont..)

- Latches are generally buffered output D-type flip-flops like 74LS373 or 8282. They are used for separating the valid address from the multiplexed address/data signals and are controlled by the ALE signal generated by 8086.
- Transreceivers are the bidirectional buffers and some times they are called as data amplifiers. They are required to separate the valid data from the time multiplexed address/data signals.
- They are controlled by two signals namely, $\overline{\text{DEN}}$ and DT/$\overline{\text{R}}$.

Minimum Mode 8086 System (cont..)

- The $\overline{\text{DEN}}$ signal indicates the direction of data, i.e. from or to the processor. The system contains memory for the monitor and users program storage.
- Usually, EPROM are used for monitor storage, while RAM for users program storage. A system may contain I/O devices.

Minimum Mode 8086 System (cont..)

- The clock generator generates the clock from the crystal oscillator and then shapes it and divides to make it more precise so that it can be used as an accurate timing reference for the system.
- The clock generator also synchronizes some external signal with the system clock. The general system organisation is as shown in below fig.
- It has 20 address lines and 16 data lines, the 8086 CPU requires three octal address latches and two octal data buffers for the complete address and data separation.

Minimum Mode 8086 System (cont..)

- The working of the minimum mode configuration system can be better described in terms of the timing diagrams rather than qualitatively describing the operations.
- The opcode fetch and read cycles are similar. Hence the timing diagram can be categorized in two parts, the first is the timing diagram for read cycle and the second is the timing diagram for write cycle.
- The read cycle begins in T_1 with the assertion of address latch enable (ALE) signal and also $M / \overline{IO}$ signal. During the negative going edge of this signal, the valid address is latched on the local bus.

Minimum Mode 8086 System (cont..)

- The $\overline{BHE}$ and $\overline{A_0}$ signals address low, high or both bytes. From T_1 to T_4 , the M/IO signal indicates a memory or I/O operation.
- At T_2, the address is removed from the local bus and is sent to the output. The bus is then tristated. The read ($\overline{RD}$) control signal is also activated in T_2.
- The read ($\overline{RD}$) signal causes the address device to enable its data bus drivers. After $\overline{RD}$ goes low, the valid data is available on the data bus.
- The addressed device will drive the READY line high. When the processor returns the read signal to high level, the addressed device will again tristate its bus drivers.

Minimum Mode 8086 System (cont..)

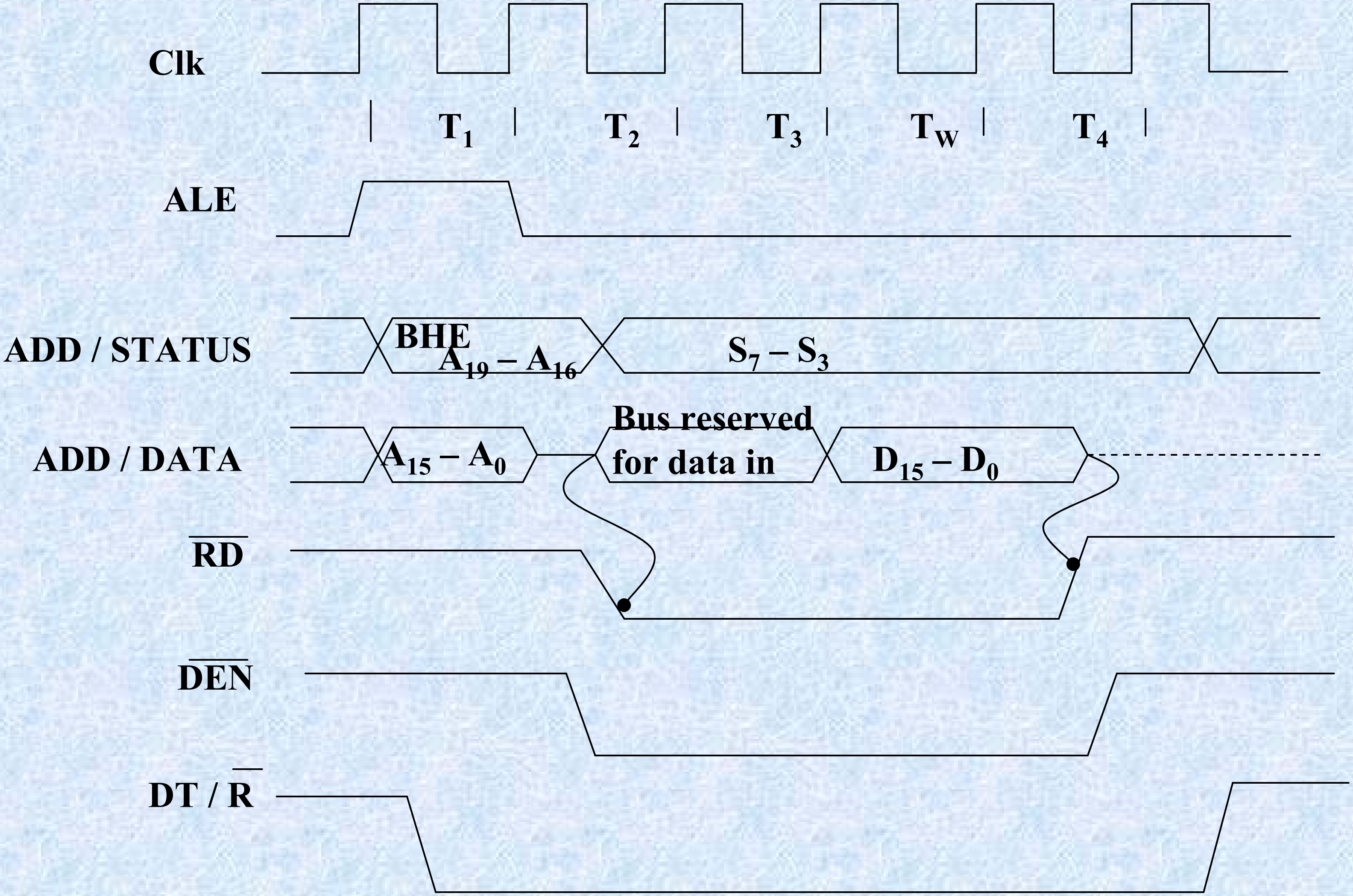
- A write cycle also begins with the assertion of ALE and the emission of the address. The $M/\overline{IO}$ signal is again asserted to indicate a memory or I/O operation. In T_2, after sending the address in T_1, the processor sends the data to be written to the addressed location.
- The data remains on the bus until middle of T_4 state. The $\overline{WR}$ becomes active at the beginning of T_2 (unlike $\overline{RD}$ is somewhat delayed in T_2 to provide time for floating).
- The $\overline{BHE}$ and A_0 signals are used to select the proper byte or bytes of memory or I/O word to be read or write.
- The $M/\overline{IO}$, $\overline{RD}$ and $\overline{WR}$ signals indicate the type of data transfer as specified in table below.

Minimum Mode 8086 System (cont..)

$M / \overline{IO}$	$\overline{RD}$	$\overline{WR}$	Transfer Type
0	0	1	I / O read
0	1	0	I/O write
1	0	1	Memory read
1	1	0	Memory write

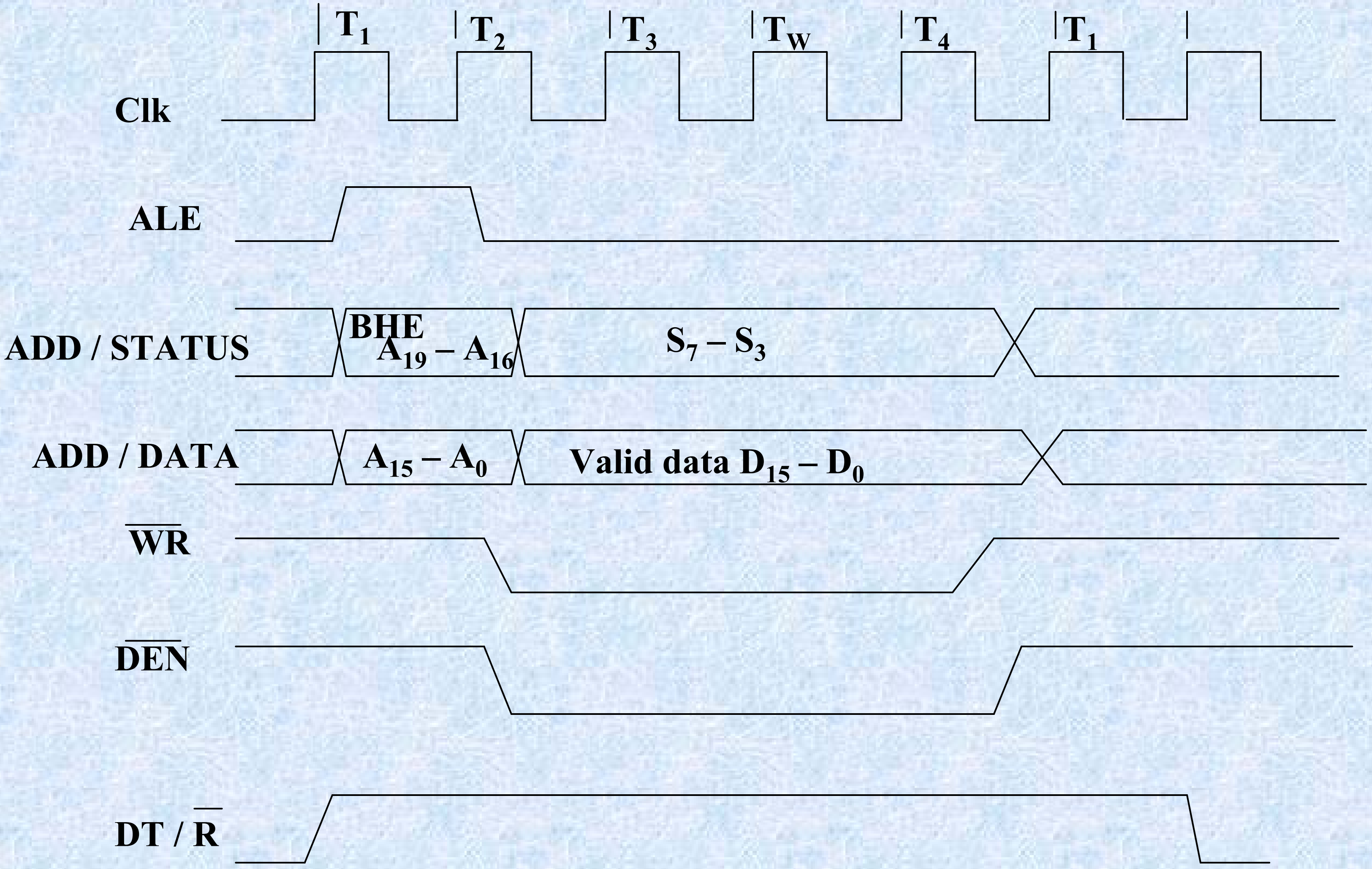
Data Transfer table

Minimum Mode 8086 System (cont..)



Read Cycle Timing Diagram for Minimum Mode

Minimum Mode 8086 System (cont..)

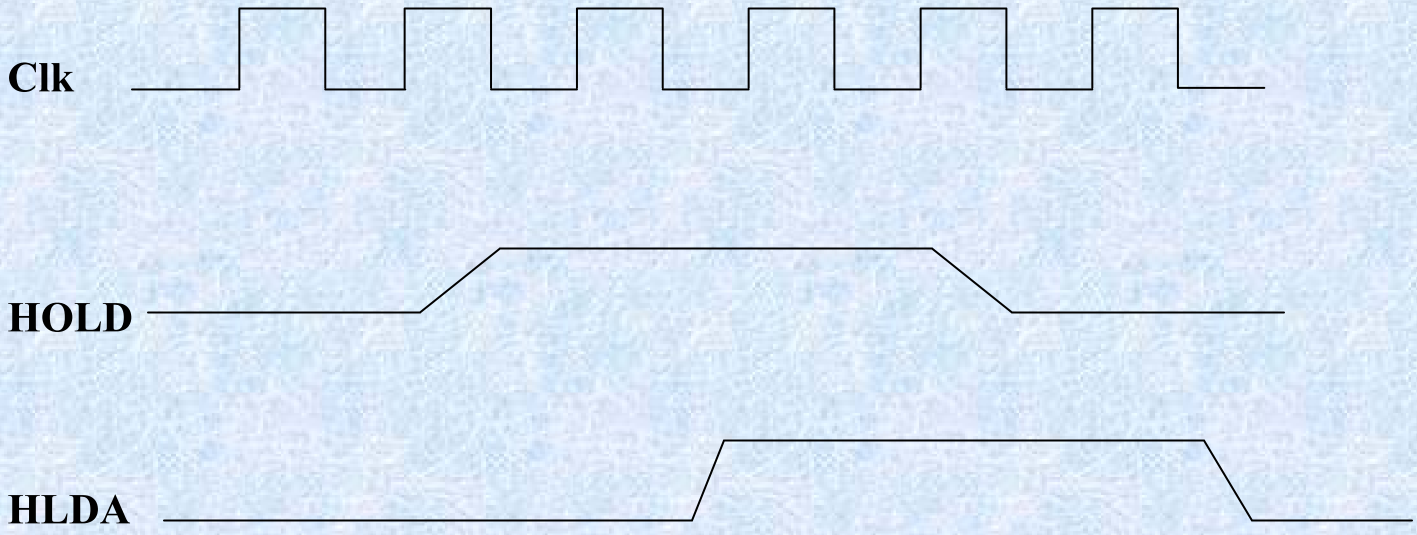


Write Cycle Timing Diagram for Minimum Mode

Minimum Mode 8086 System (cont..)

- ***Hold Response sequence***: The HOLD pin is checked at leading edge of each clock pulse. If it is received active by the processor before T_4 of the previous cycle or during T_1 state of the current cycle, the CPU activates HLDA in the next clock cycle and for succeeding bus cycles, the bus will be given to another requesting master.
- The control of the bus is not regained by the processor until the requesting master does not drop the HOLD pin low. When the request is dropped by the requesting master, the HLDA is dropped by the processor at the trailing edge of the next clock.

Minimum Mode 8086 System (cont..)



Bus Request and Bus Grant Timings in Minimum Mode System

Maximum Mode 8086 System

- In the maximum mode, the 8086 is operated by strapping the MN/$\overline{\text{MX}}$ pin to ground.
- In this mode, the processor derives the status signal $\overline{S}_2$, $\overline{S}_1$, $\overline{S}_0$. Another chip called bus controller derives the control signal using this status information .
- In the maximum mode, there may be more than one microprocessor in the system configuration.
- The components in the system are same as in the minimum mode system.

Maximum Mode 8086 System (cont..)

- The basic function of the bus controller chip IC8288, is to derive control signals like RD and WR (for memory and I/O devices), $\overline{DEN}$, DT/$\overline{R}$, ALE etc. using the information by the processor on the status lines.
- The bus controller chip has input lines $\overline{S}_2$, $\overline{S}_1$, $\overline{S}_0$ and CLK. These inputs to 8288 are driven by CPU.
- It derives the outputs ALE, $\overline{DEN}$, DT/$\overline{R}$, $\overline{MRDC}$, $\overline{MWTC}$, $\overline{AMWC}$, $\overline{IORC}$, $\overline{IOWC}$ and $\overline{AIOWC}$. The $\overline{AEN}$, IOB and CEN pins are specially useful for multiprocessor systems.

Maximum Mode 8086 System (cont..)

- AEN and $\overline{\text{IOB}}$ are generally grounded. CEN pin is usually tied to +5V. The significance of the MCE/$\overline{\text{PDEN}}$ output depends upon the status of the IOB pin.
- If IOB is grounded, it acts as master cascade enable to control cascade 8259A, else it acts as peripheral data enable used in the multiple bus configurations.
- $\overline{\text{INTA}}$ pin used to issue two interrupt acknowledge pulses to the interrupt controller or to an interrupting device.

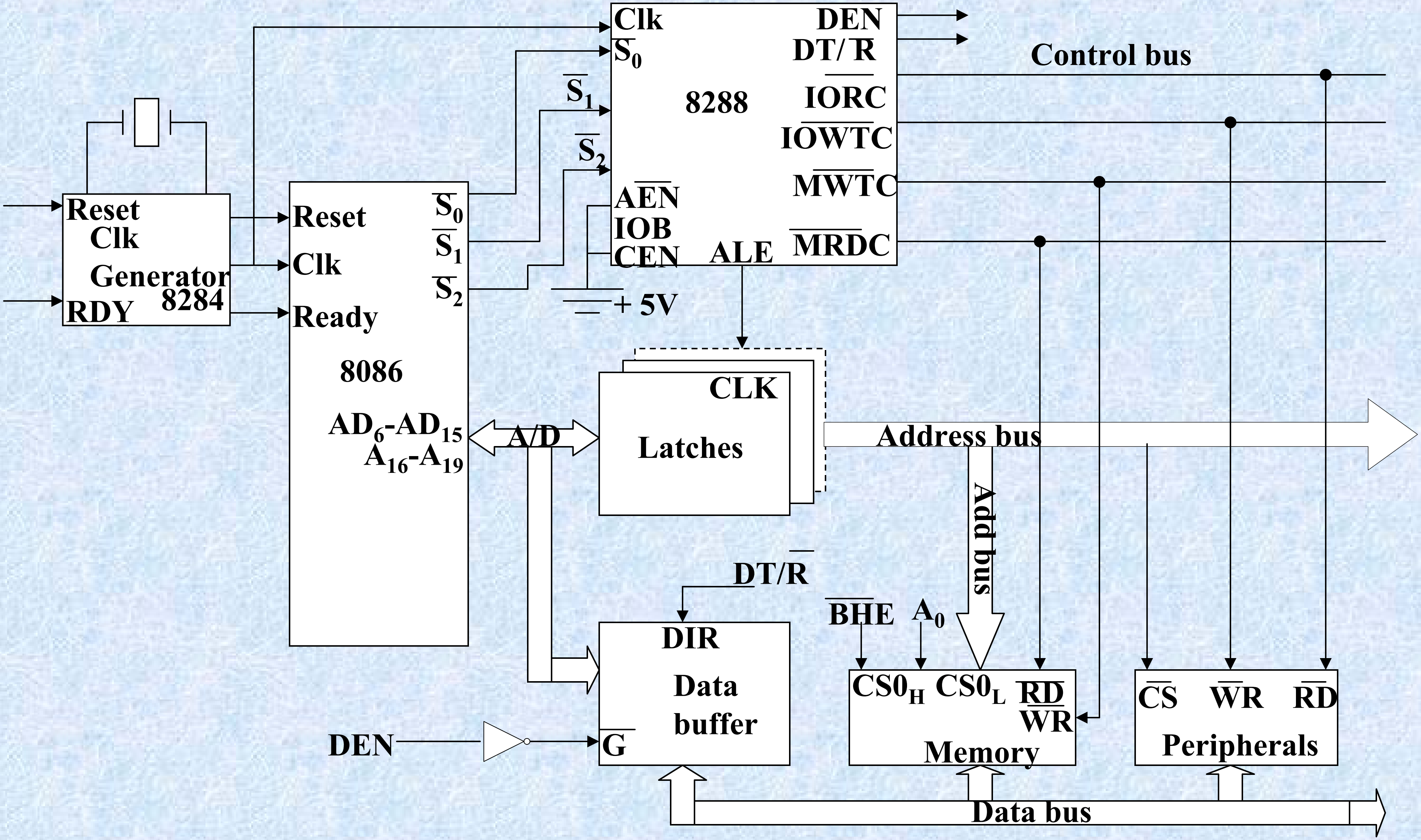
Maximum Mode 8086 System (cont..)

- $\overline{\text{IORC}}$, $\overline{\text{IOWC}}$ are I/O read command and I/O write command signals respectively . These signals enable an IO interface to read or write the data from or to the address port.
- The $\overline{\text{MRDC}}$, $\overline{\text{MWTC}}$ are memory read command and memory write command signals respectively and may be used as memory read or write signals.
- All these command signals instructs the memory to accept or send data from or to the bus.
- For both of these write command signals, the advanced signals namely $\overline{\text{AIOWC}}$ and $\overline{\text{AMWTC}}$ are available.

Maximum Mode 8086 System (cont..)

- They also serve the same purpose, but are activated one clock cycle earlier than the $\overline{\text{IOWC}}$ and $\overline{\text{MWTC}}$ signals respectively.
- The maximum mode system timing diagrams are divided in two portions as read (input) and write (output) timing diagrams.
- The address/data and address/status timings are similar to the minimum mode.
- ALE is asserted in T_1, just like minimum mode. The only difference lies in the status signal used and the available control and advanced command signals.

Maximum Mode 8086 System (cont..)



Maximum Mode 8086 System.

Maximum Mode 8086 System (cont..)

- Here the only difference between in timing diagram between minimum mode and maximum mode is the status signals used and the available control and advanced command signals.
- $\overline{R_0}$, $\overline{S_1}$, $\overline{S_2}$ are set at the beginning of bus cycle.8288 bus controller will output a pulse as on the ALE and apply a required signal to its DT / R pin during T_1.

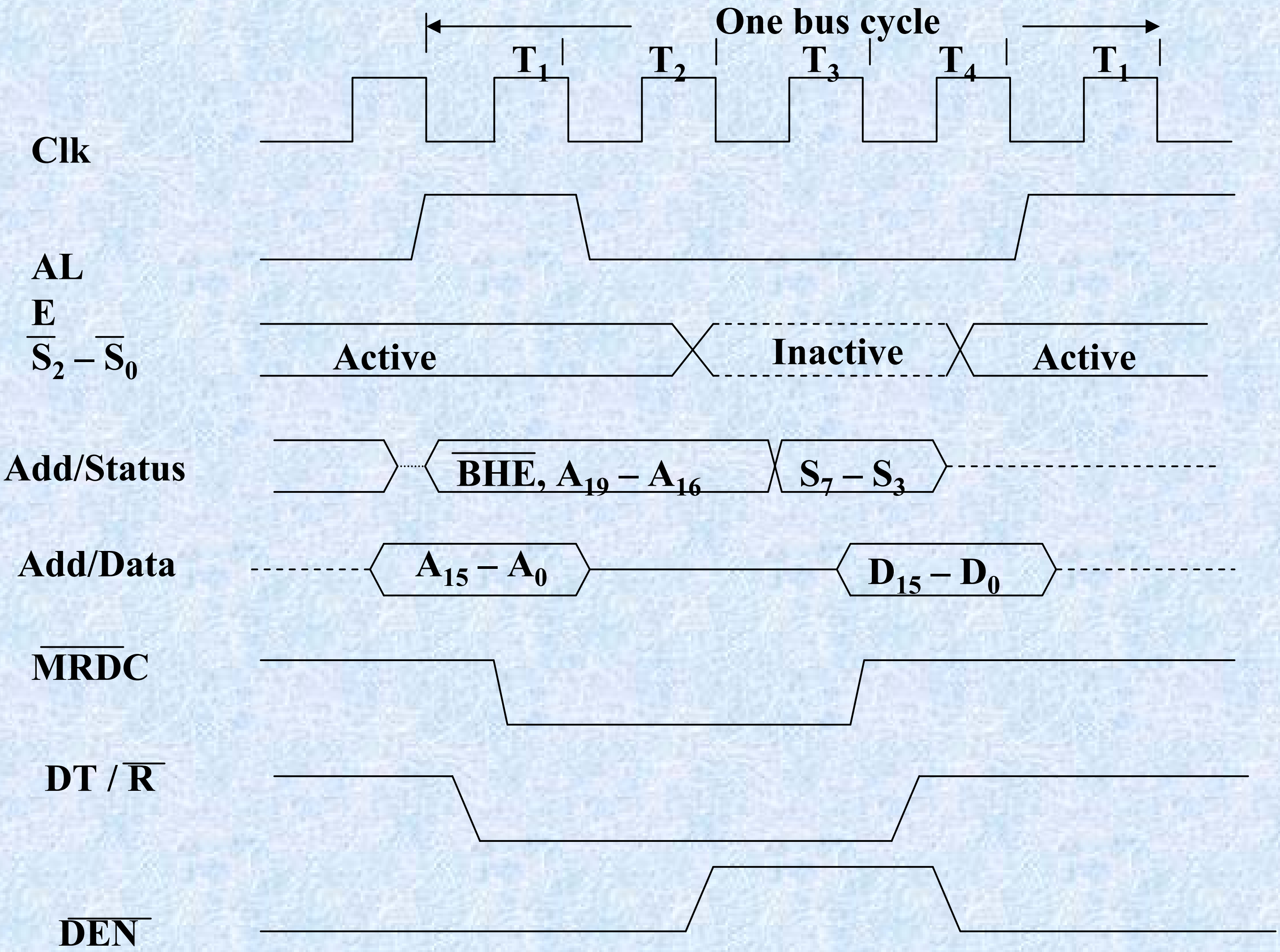
Maximum Mode 8086 System (cont..)

- In T_2, 8288 will set $\overline{DEN}$=1 thus enabling transceivers, and for an input it will activate $\overline{MRDC}$ or $\overline{IORC}$. These signals are activated until T_4. For an output, the $\overline{AMWC}$ or $A\overline{IOWC}$ is activated from T_2 to T_4 and $\overline{MWTC}$ or $\overline{IOWC}$ is activated from T_3 to T_4.
- The status bit S_0 to S_2 remains active until T_3 and become passive during T_3 and T_4.
- If reader input is not activated before T_3, wait state will be inserted between T_3 and T_4.

Maximum Mode 8086 System (cont..)

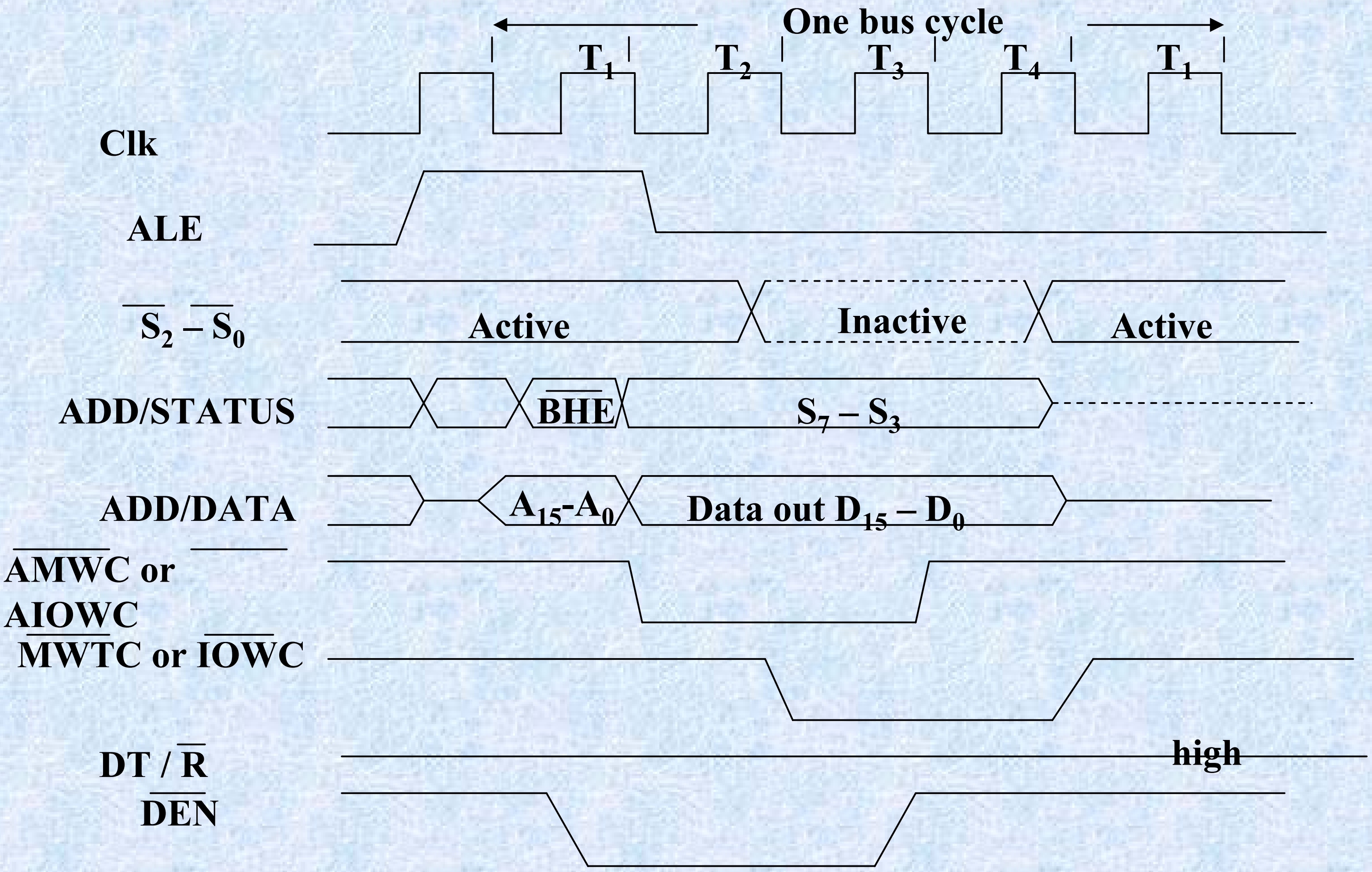
- **Timings for $\overline{RQ}/\overline{GT}$ Signals :**The request/grant response sequence contains a series of three pulses. The request/grant pins are checked at each rising pulse of clock input.
- When a request is detected and if the condition for HOLD request are satisfied, the processor issues a grant pulse over the $\overline{RQ}/\overline{GT}$ pin immediately during T_4 (current) or T_1 (next) state.
- When the requesting master receives this pulse, it accepts the control of the bus, it sends a release pulse to the processor using $\overline{RQ}/\overline{GT}$ pin.

Maximum Mode 8086 System (cont..)



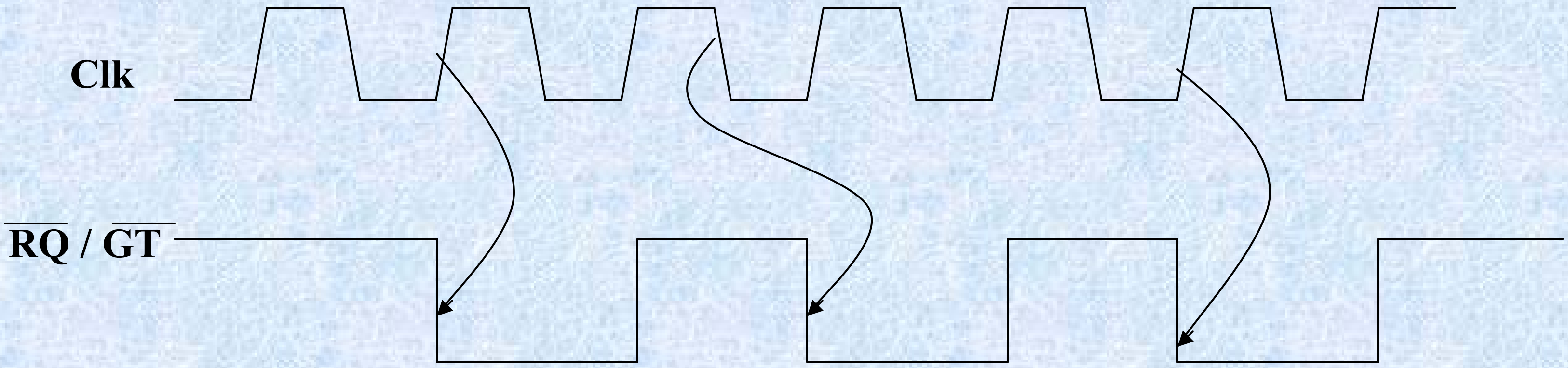
Memory Read Timing in Maximum Mode

Maximum Mode 8086 System (cont..)



Memory Write Timing in Maximum mode.

Maximum Mode 8086 System (cont..)



Another master request bus access

CPU grant bus

Master releases bus

$\overline{RQ}/\overline{GT}$ Timings in Maximum Mode.

Internal Registers of 8086 (cont..)

- The 8086 has four groups of the user accessible internal registers. They are the instruction pointer, four data registers, four pointer and index register, four segment registers.
- The 8086 has a total of fourteen 16-bit registers including a 16 bit register called the ***status register***, with 9 of bits implemented for status and control flags.

Internal Registers of 8086 (cont..)

- Most of the registers contain data/instruction offsets within 64 KB memory segment. There are four different 64 KB segments for instructions, stack, data and extra data. To specify where in 1 MB of processor memory these 4 segments are located the processor uses four segment registers:
- **Code segment** (CS) is a 16-bit register containing address of 64 KB segment with processor instructions. The processor uses CS segment for all accesses to instructions referenced by instruction pointer (IP) register. CS register cannot be changed directly. The CS register is automatically updated during far jump, far call and far return instructions.

Internal Registers of 8086 (cont..)

- **Stack segment** (SS) is a 16-bit register containing address of 64KB segment with program stack. By default, the processor assumes that all data referenced by the stack pointer (SP) and base pointer (BP) registers is located in the stack segment. SS register can be changed directly using POP instruction.
- **Data segment** (DS) is a 16-bit register containing address of 64KB segment with program data. By default, the processor assumes that all data referenced by general registers (AX, BX, CX, DX) and index register (SI, DI) is located in the data segment. DS register can be changed directly using POP and LDS instructions.

Internal Registers of 8086 (cont..)

- **Extra segment** (ES) is a 16-bit register containing address of 64KB segment, usually with program data. By default, the processor assumes that the DI register references the ES segment in string manipulation instructions. ES register can be changed directly using POP and LES instructions.
- It is possible to change default segments used by general and index registers by prefixing instructions with a CS, SS, DS or ES prefix.
- All general registers of the 8086 microprocessor can be used for arithmetic and logic operations. The general registers are:

Internal Registers of 8086 (cont..)

- **Accumulator** register consists of two 8-bit registers AL and AH, which can be combined together and used as a 16-bit register AX. AL in this case contains the low-order byte of the word, and AH contains the high-order byte. Accumulator can be used for I/O operations and string manipulation.
- **Base** register consists of two 8-bit registers BL and BH, which can be combined together and used as a 16-bit register BX. BL in this case contains the low-order byte of the word, and BH contains the high-order byte. BX register usually contains a data pointer used for based, based indexed or register indirect addressing.

Internal Registers of 8086 (cont..)

- **Count** register consists of two 8-bit registers CL and CH, which can be combined together and used as a 16-bit register CX. When combined, CL register contains the low-order byte of the word, and CH contains the high-order byte. Count register can be used in Loop, shift/rotate instructions and as a counter in string manipulation,.
- **Data** register consists of two 8-bit registers DL and DH, which can be combined together and used as a 16-bit register DX. When combined, DL register contains the low-order byte of the word, and DH contains the high-order byte. Data register can be used as a port number in I/O operations. In integer 32-bit multiply and divide instruction the DX register contains high-order word of the initial or resulting number.

Internal Registers of 8086 (cont..)

- The following registers are both general and index registers:
- **Stack Pointer** (SP) is a 16-bit register pointing to program stack.
- **Base Pointer** (BP) is a 16-bit register pointing to data in stack segment. BP register is usually used for based, based indexed or register indirect addressing.
- **Source Index** (SI) is a 16-bit register. SI is used for indexed, based indexed and register indirect addressing, as well as a source data address in string manipulation instructions.

Internal Registers of 8086 (cont..)

- **Destination Index** (DI) is a 16-bit register. DI is used for indexed, based indexed and register indirect addressing, as well as a destination data address in string manipulation instructions.

Other registers:

- **Instruction Pointer** (IP) is a 16-bit register.
- **Flags** is a 16-bit register containing 9 one bit flags.
- **Overflow Flag** (OF) - set if the result is too large positive number, or is too small negative number to fit into destination operand.

Internal Registers of 8086 (cont..)

- **Direction Flag** (DF) - if set then string manipulation instructions will auto-decrement index registers. If cleared then the index registers will be auto-incremented.
- **Interrupt-enable Flag** (IF) - setting this bit enables maskable interrupts.
- **Single-step Flag** (TF) - if set then single-step interrupt will occur after the next instruction.
- **Sign Flag** (SF) - set if the most significant bit of the result is set.
- **Zero Flag** (ZF) - set if the result is zero.

Internal Registers of 8086

- **Auxiliary carry Flag** (AF) - set if there was a carry from or borrow to bits 0-3 in the AL register.
- **Parity Flag** (PF) - set if parity (the number of "1" bits) in the low-order byte of the result is even.
- **Carry Flag** (CF) - set if there was a carry from or borrow to the most significant bit during last result calculation.

Addressing Modes (cont..)

- **Implied -** the data value/data address is implicitly associated with the instruction.
- **Register -** references the data in a register or in a register pair.
- **Immediate** - the data is provided in the instruction.
- **Direct -** the instruction operand specifies the memory address where data is located.
- **Register indirect -** instruction specifies a register containing an address, where data is located. This addressing mode works with SI, DI, BX and BP registers.
- **Based** :- 8-bit or 16-bit instruction operand is added to the contents of a base register (BX or BP), the resulting value is a pointer to location where data resides.

Addressing Modes

- **Indexed** :- 8-bit or 16-bit instruction operand is added to the contents of an index register (SI or DI), the resulting value is a pointer to location where data resides.
- **Based Indexed** :- the contents of a base register (BX or BP) is added to the contents of an index register (SI or DI), the resulting value is a pointer to location where data resides.
- **Based Indexed with displacement** :- 8-bit or 16-bit instruction operand is added to the contents of a base register (BX or BP) and index register (SI or DI), the resulting value is a pointer to location where data resides.

Memory (cont..)

- Program, data and stack memories occupy the same memory space. As the most of the processor instructions use 16-bit pointers the processor can effectively address only 64 KB of memory.
- To access memory outside of 64 KB the CPU uses special segment registers to specify where the code, stack and data 64 KB segments are positioned within 1 MB of memory (see the "Registers" section below).
- 16-bit pointers and data are stored as:
  address: low-order byte
  address+1: high-order byte

Memory (cont..)

- 32-bit addresses are stored in "segment: offset" format as:
  address: low-order byte of segment
  address+1: high-order byte of segment
  address+2: low-order byte of offset
  address+3: high-order byte of offset
- Physical memory address pointed by segment: offset pair is calculated as:
- address = (<segment> * 16) + <offset>

Memory (cont..)

- **Program memory -** program can be located anywhere in memory. Jump and call instructions can be used for short jumps within currently selected 64 KB code segment, as well as for far jumps anywhere within 1 MB of memory.
- All conditional jump instructions can be used to jump within approximately +127 to -127 bytes from current instruction.
- **Data memory -** the processor can access data in any one out of 4 available segments, which limits the size of accessible memory to 256 KB (if all four segments point to different 64 KB blocks).

Memory (cont..)

- Accessing data from the Data, Code, Stack or Extra segments can be usually done by prefixing instructions with the DS:, CS:, SS: or ES: (some registers and instructions by default may use the ES or SS segments instead of DS segment).
- Word data can be located at odd or even byte boundaries. The processor uses two memory accesses to read 16-bit word located at odd byte boundaries. Reading word data from even byte boundaries requires only one memory access.

Memory

- **Stack memory** can be placed anywhere in memory. The stack can be located at odd memory addresses, but it is not recommended for performance reasons (see "Data Memory" above).

Reserved locations:

- 0000h - 03FFh are reserved for interrupt vectors. Each interrupt vector is a 32-bit pointer in format segment: offset.
- FFFF0h - FFFFFh - after RESET the processor always starts program execution at the FFFF0h address.

Interrupts (cont..)

The processor has the following interrupts:

- **INTR** is a maskable hardware interrupt. The interrupt can be enabled/disabled using STI/CLI instructions or using more complicated method of updating the FLAGS register with the help of the POPF instruction.
- When an interrupt occurs, the processor stores FLAGS register into stack, disables further interrupts, fetches from the bus one byte representing interrupt type, and jumps to interrupt processing routine address of which is stored in location 4 * <interrupt type>. Interrupt processing routine should return with the IRET instruction.

Interrupts (cont..)

- **NMI** is a non-maskable interrupt. Interrupt is processed in the same way as the INTR interrupt. Interrupt type of the NMI is 2, i.e. the address of the NMI processing routine is stored in location 0008h. This interrupt has higher priority then the maskable interrupt.
- **Software interrupts** can be caused by:
- INT instruction - breakpoint interrupt. This is a type 3 interrupt.
- INT <interrupt number> instruction - any one interrupt from available 256 interrupts.
- INTO instruction - interrupt on overflow

Interrupts

- Single-step interrupt - generated if the TF flag is set. This is a type 1 interrupt. When the CPU processes this interrupt it clears TF flag before calling the interrupt processing routine.
- **Processor exceptions**: Divide Error (Type 0), Unused Opcode (type 6) and Escape opcode (type 7).
- Software interrupt processing is the same as for the hardware interrupts.