1. In 8051 an external interrupt 1 vector address is of _____ and causes of interrupt if ____.
a) 000BH, a high to low transition on pin INT1
b) 001BH, a low to high transition on pin INT1
c) 0013H, a high to low transition on pin INT1
d) 0023H, a low to high transition on pin INT1

2. Serial port vector address is of _____. And causes an interrupt when _____.
a) 0013H, either TI or RI flag is set
b) 0023H, either TI or RI flag is reset
c) 0013H, either TI or RI flag is reset
d) 0023H, either TI or RI flag is set

3. In serial communication modes, mode 1 the Baud rate =
a) BR=2^{SMOD}/32 * (Timer 0 over flow rate)
b) BR=2^{SMOD}/16 * (Timer 1 over flow rate)
c) BR=2^{SMOD}/16 * (Timer 0 over flow rate)
d) BR=2^{SMOD}/32 * (Timer 1 over flow rate)
4. In modes 2 and 3, if _____ bit of SCON bit is set will causes enable multiprocessor communication and is of ____ bit address.
a) SM1, 9EH   b) TB8 , 9CH   c) SM2, 9DH   d) SM0, 9FH
5. Interfacing LCD with 89C51 _____ data lines are used along with the _____ signals.
a) 6, RS, RW   b) 5, RW, EN   c) 8, RS, EN, RW   d) 9, RS, EN, RW
6. Resolution of ADC is defined as
a) $1/(2N-1)$ b) $2^{N}-1$ c) $1/(2^{N}-1)$ d) 2N-1
7. In microcontroller and LCD interface which line will instruct the LCD that microcontroller is sending data?
a) DB0 b) RW c) EN   d) RS
8. Which bit of TMOD will exactly configure timer / counter as a timer or counter.
 i) TMOD.6 of C/T for timer 1   ii) TMOD.6 of C/T for timer 0
 iii) TMOD.2 of C/T for timer 0   iv) TMOD.2 of C/T for timer 1
a) i, ii   b) ii, iv c) i, iii d) iii, iv

Key:

7.1 C   7.2 D   7.3 D   7.4 C   7.5 C   7.6 C   7.7 C   7.8 C