

Design Verification and Test of
Digital VLSI Circuits
NPTEL Video Course

Module-X

Lecture-I

**ATPG for Synchronous Sequential
Circuits**

Introduction

- VLSI testing, only from the context of combinational circuits (last 3 modules)
- ATPG for sequential circuits.
 - variations required in fault model, algebra and ATPG procedure
 - compare the ATPG Complexity
 - A special scheme called “scan chain” which “modifies a sequential circuit into a virtual combinational one”.

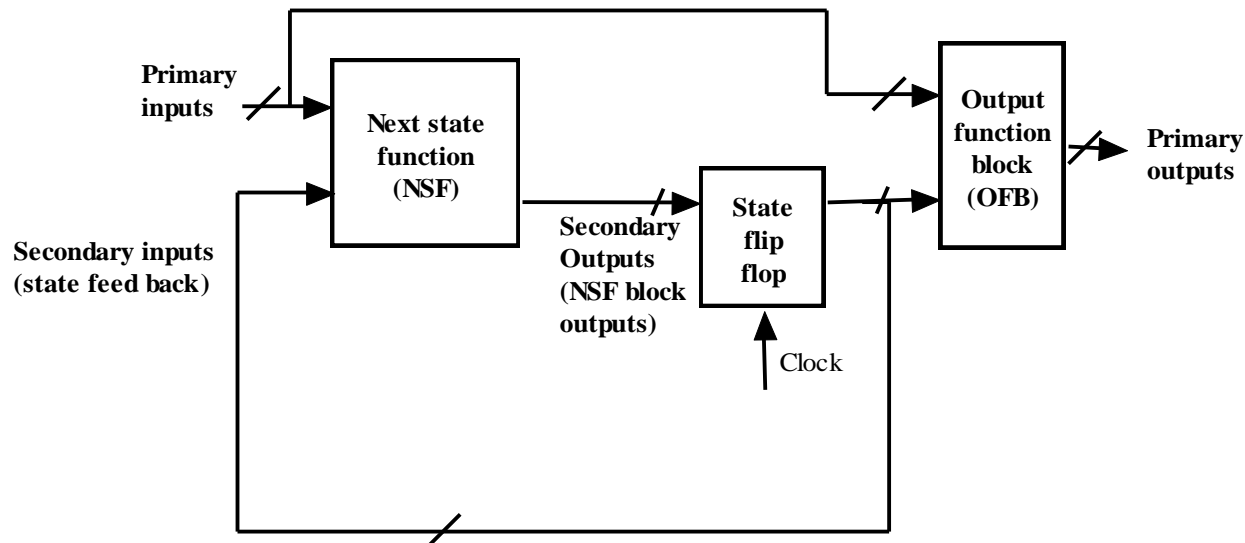
So, test patterns for a sequential circuit with scan chain can be generated with slight variation in ATPG algorithms for combinational circuits (D-algorithm, for example).

ATPG and testing: Sequential versus combinational circuits

- Basic architecture of a sequential circuit

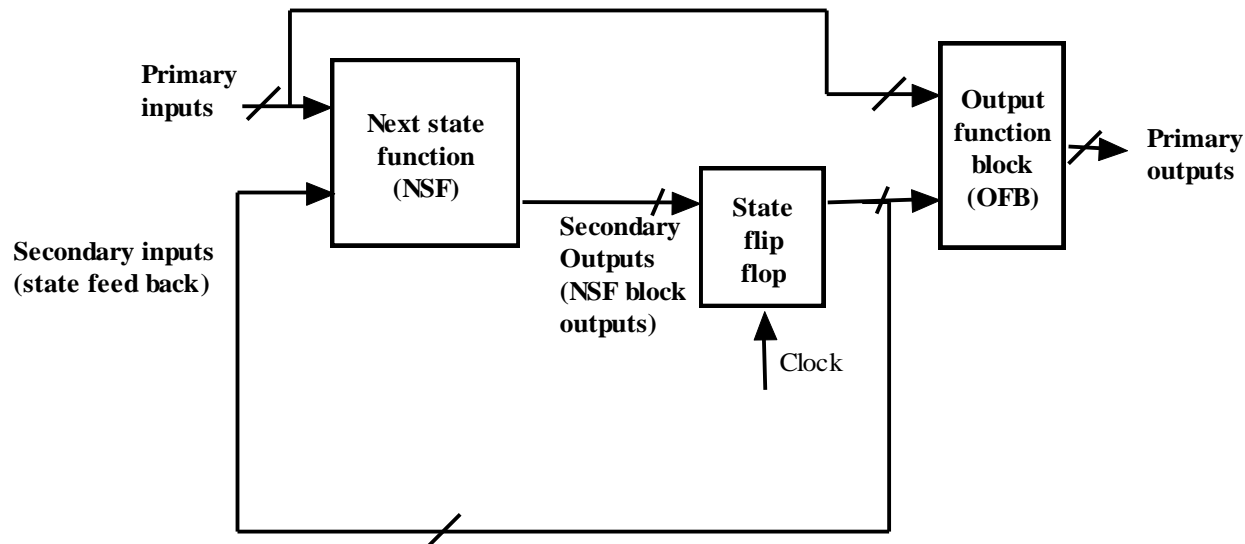
NSF (Combinational), OFB (Combinational), and state flip-flop (sequential).

- ATPG procedure for the NSF and OFB blocks similar to combinational circuits.
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- Compared to a standard combinational circuit, in case of NSF/OBF some inputs (state feedback) are not controllable/its outputs are not observable.



ATPG and testing: Sequential versus combinational circuits

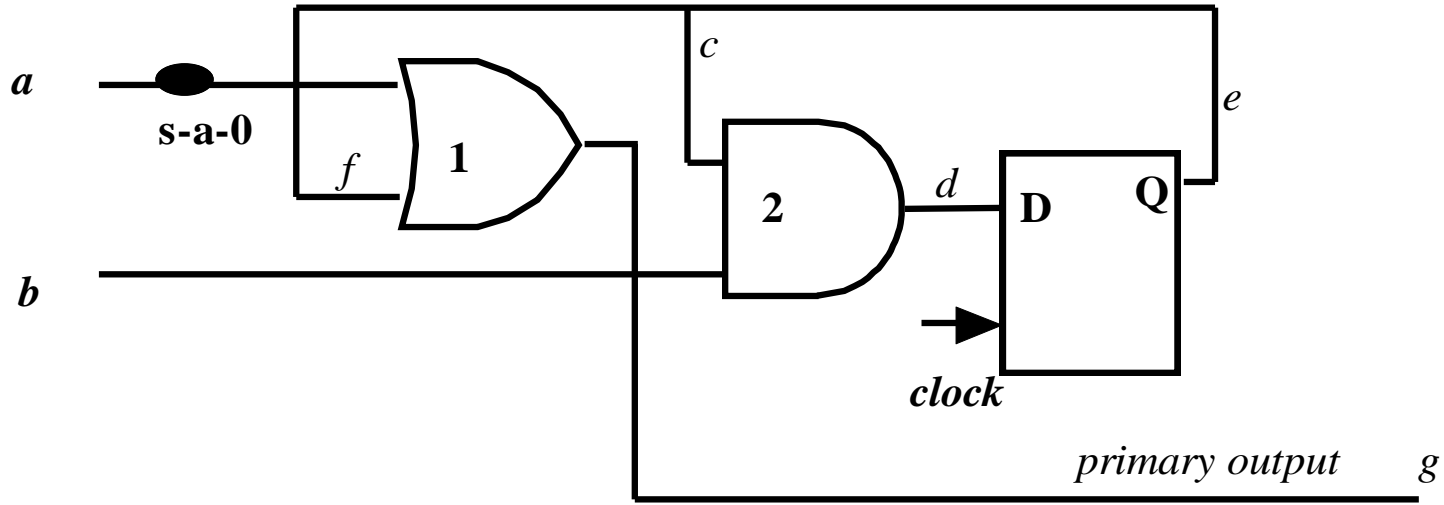
- When a circuit powers up, the flip-flops can have any value (0 or 1).
- ATPG need to control (indirectly) the outputs of flip-flops and observe (indirectly) the inputs to the flip-flops.
- Once achieved, ATPG for these combinational blocks can be done using D-algorithm.



ATPG of sequential circuits: Assumptions

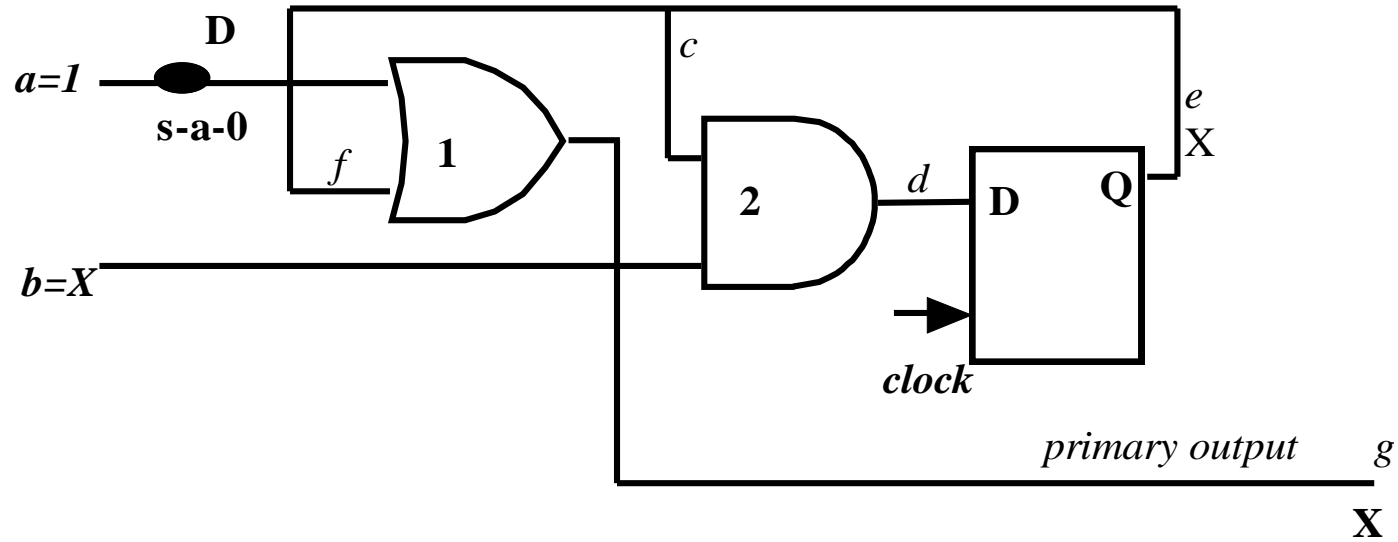
- Single clock sequential circuits.
- Each flip-flop is treated as 1-bit memory element with ONE common clock.
- After a clock edge, the secondary output pattern (next state) is transferred to the output of the flip-flops (present state), which become new secondary inputs. Also, the primary outputs are updated. This activity occurs at each clock edge, and so it is called “synchronous” operation.
- Single stuck at faults are assumed in NSF and OFB.
- Internal faults of flip-flops are not modeled; their output and input faults are modeled as faults on input and output signals of the combinational blocks.
- No faults are considered in the clock signal.
- Most of the time, D-flip-flops are used in VLSI designs. So in this course whenever we refer to a flip-flop we essentially mean a D-flip-flop.

ATPG of sequential circuits: Example



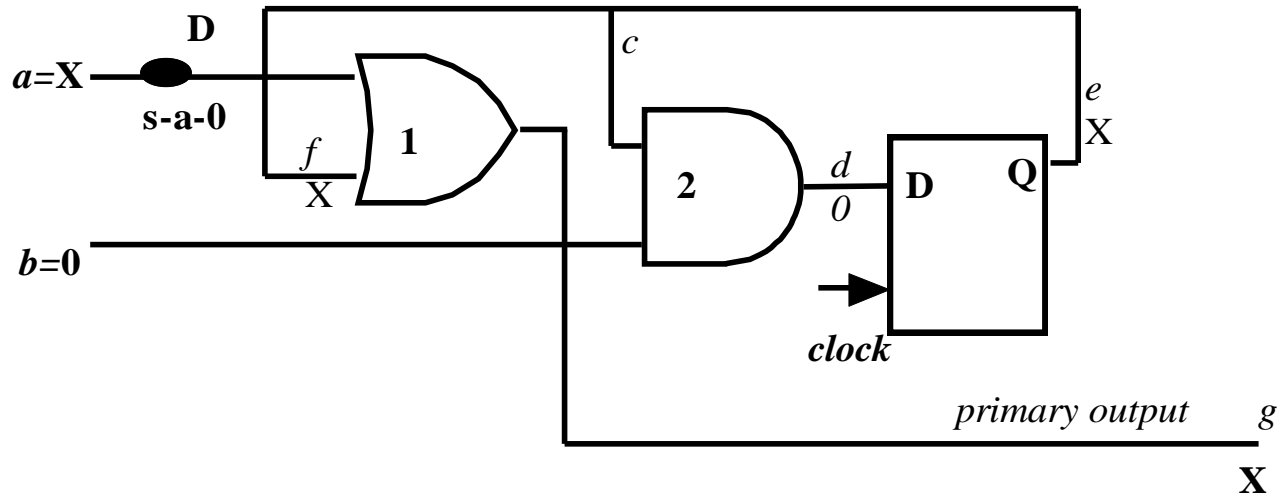
A simple sequential circuit with a stuck-at-0 fault

ATPG of sequential circuits: Example



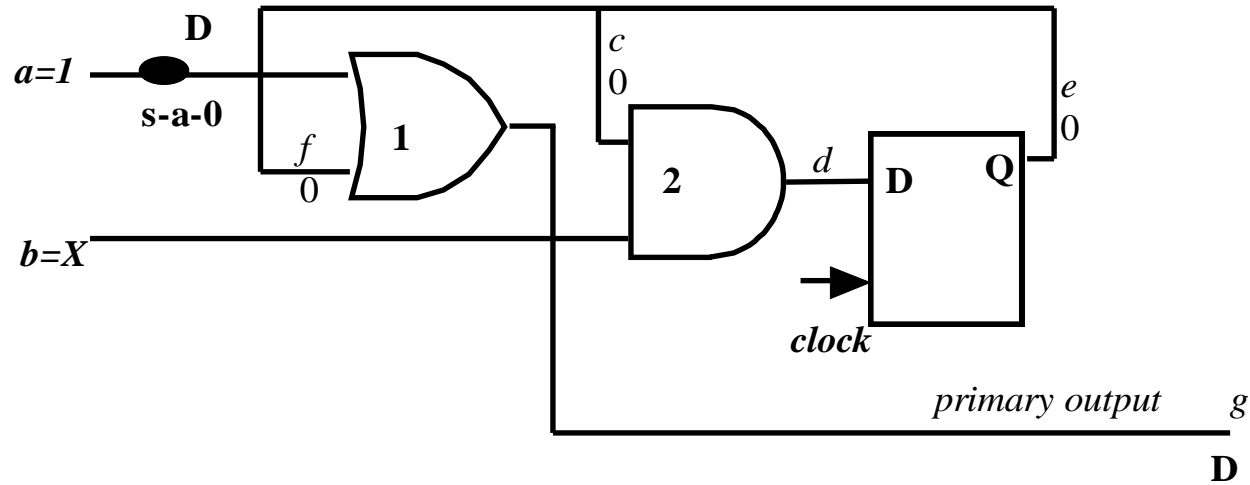
Problems in ATPG for the stuck-at-0 fault

ATPG of sequential circuits: Example



Indirect controlling of f to 0

ATPG of sequential circuits: Example



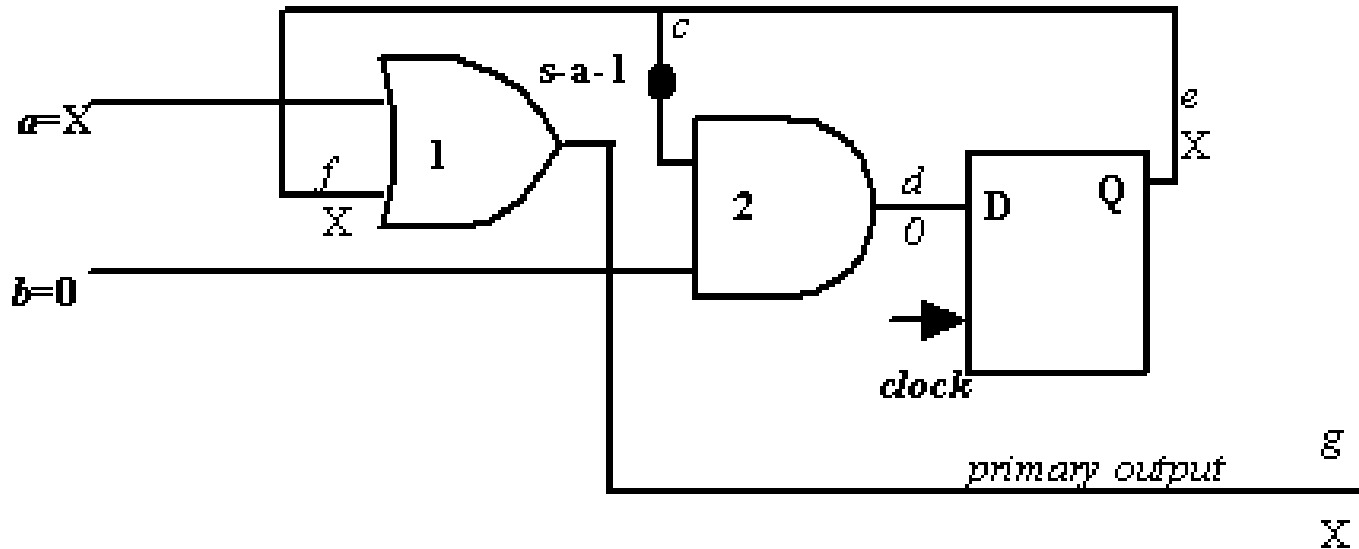
Test pattern for the s-a-0 fault

ATPG for combinational blocks in sequential circuits require more than one pattern. In this example, the first pattern is $a=X$, $b=0$ and clock edge followed by $a=1$ and $b=X$.

Final pattern is according to combinational ATPG (that sensitize the fault and propagates the effect to a primary output) and all other initial patterns are to bring the secondary inputs to their required value.

ATPG of sequential circuits: Example

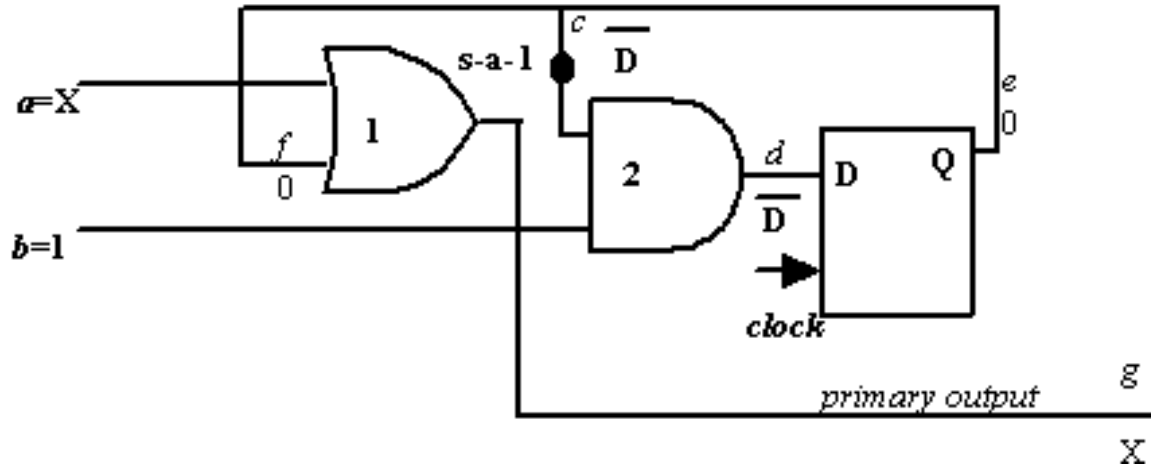
Fault in NSF



- ATPG for a fault in the NSF block is more complex than the ones in the OFB.
- In case of a fault in the NSF we need to indirectly control the secondary inputs and in addition, propagate the fault effect to the primary output via OFB.
- First, primary input $b=0$ ($a=X$) and a clock edge is applied; this makes $e=0$ (and also $c=0$) after the edge.

ATPG of sequential circuits: Example

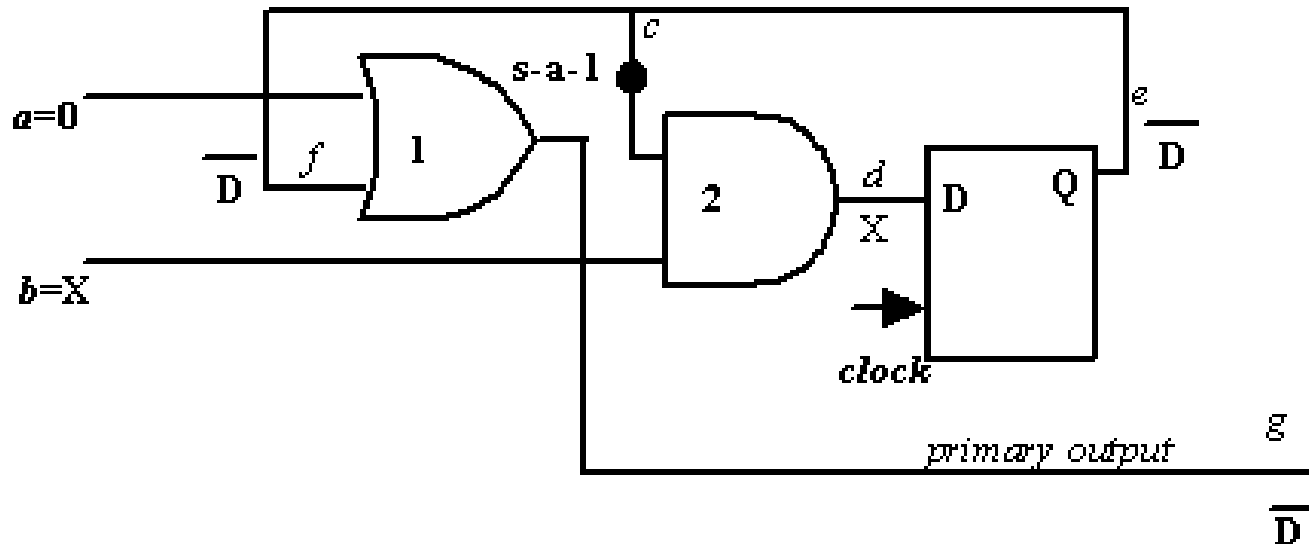
Fault in NSF



- Even in presence of the s-a-1 fault, $b=0$ and a clock edge makes $c=0$; this sensitizes the fault (\bar{d} at c).
- In the next step, $b=1$ ($a=X$) and a clock edge would propagate the fault effect (\bar{d}) to the output of the flip-flop (i.e, secondary input of the OFB).

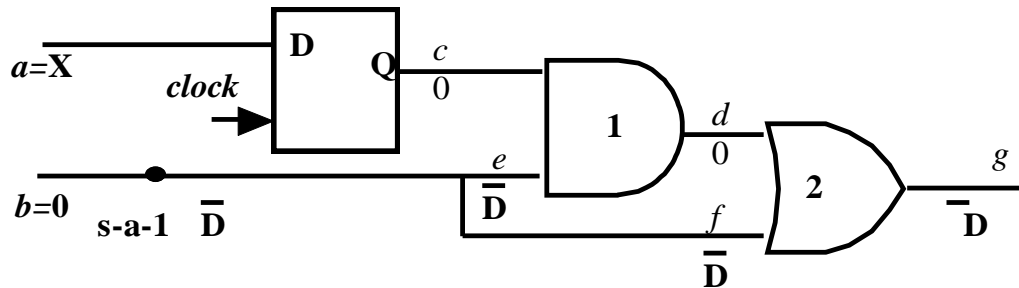
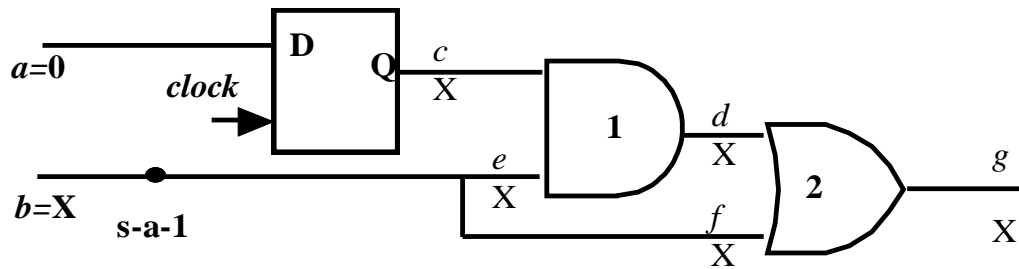
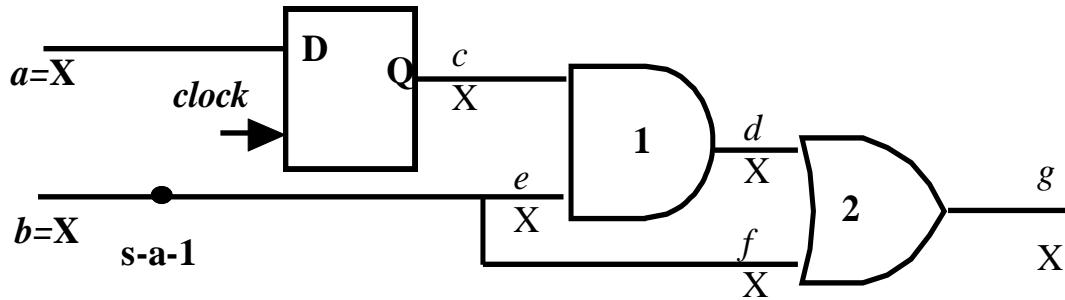
ATPG of sequential circuits: Example

Fault in NSF



- Finally, $a=0$ ($b=X$) would propagate fault effect to the primary output.

Algebra for ATPG of sequential circuits



Fault effect propagate by two paths “ $e-d-g$ ” or “ $f-g$ ”, taken ($f-g$).

- Need net $d=0$.
- Need to apply 0 at b .

- Net d is not directly controllable, need to make $a=0$ ($b=X$) and apply a clock pulse.

- Next apply $b=0$ ($a=X$), the fault effect \overline{D} would appear in the primary output.

Algebra for ATPG of sequential circuits

- In the example, higher order algebra is used, as a net is marked as 0/X, which is not available in 5 value algebra.
- Higher order algebra improves efficiency of ATPG of sequential circuits. As higher order algebra reduces the number of input (primary and secondary) lines to be controlled, there is reduction in the number of steps (in terms of clock edges and test patterns) to control the secondary inputs (or make the NSF block outputs observable via OFB). However, it does not guarantee that ATPG will not require controlling the secondary inputs and propagating the fault effect to the primary output via OFB. This example was a special case where controlling the secondary inputs were not required.
- Higher order algebra will also reduce the number of lines to be controlled in ATPG of a combinational circuit. However, it is not applied as computational complexity rises with increase in order of the algebra and inputs are easily controllable in combinational circuits.

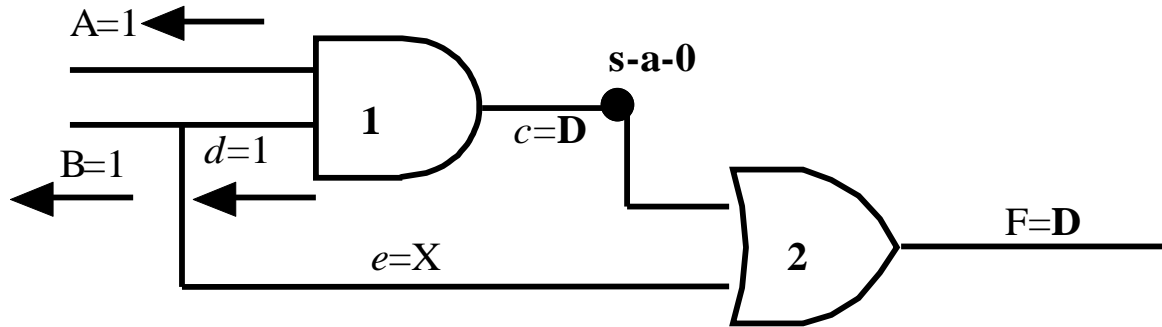
Algebra for ATPG of sequential circuits

Nine value algebra

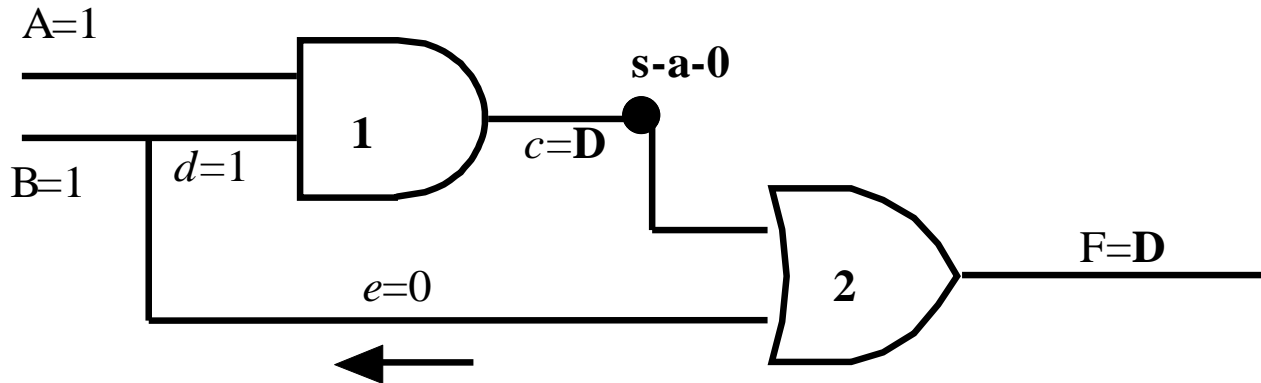
Symbol	Implication	Normal Circuit	Faulty Circuit
0	(0/0)	0	0
1	(1/1)	1	1
X	(X/X)	X	X
D	(1/0)	1	0
\bar{D}	(0/1)	0	1
G0	(0/X)	0	X
G1	(1/X)	1	X
F0	(X/0)	X	0
F1	(X/1)	X	1

Questions and Answers

Answer



D-frontier = {}
Backward Implication



Backward Implication
Inconstancy

Thank You

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Module-X

Lecture-II

**Scan Chain based Sequential
Circuit Testing**

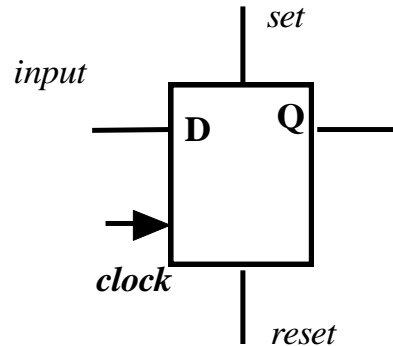
Introduction

- The major problem in testing (and ATPG) of sequential circuits is difficulty in controlling secondary inputs (i.e., outputs of flip-flops) and difficulty in observing secondary outputs (i.e., inputs of flip-flops).
 - Sequence of patterns for ATPG of a fault
- In this lecture we will discuss various techniques to make the flip-flops controllable and observable, which convert a sequential circuit into virtual combinational one.
 - ATPG for combinational circuits would suffice for sequential circuits.
 - However, for achieving this, additional circuitry, called design for test (DFT), will be put on-chip, which would add to extra area overhead.
- Explore different schemes to control and observe the flip-flops.

Controllability and observability of flip-flops

•Set and reset lines

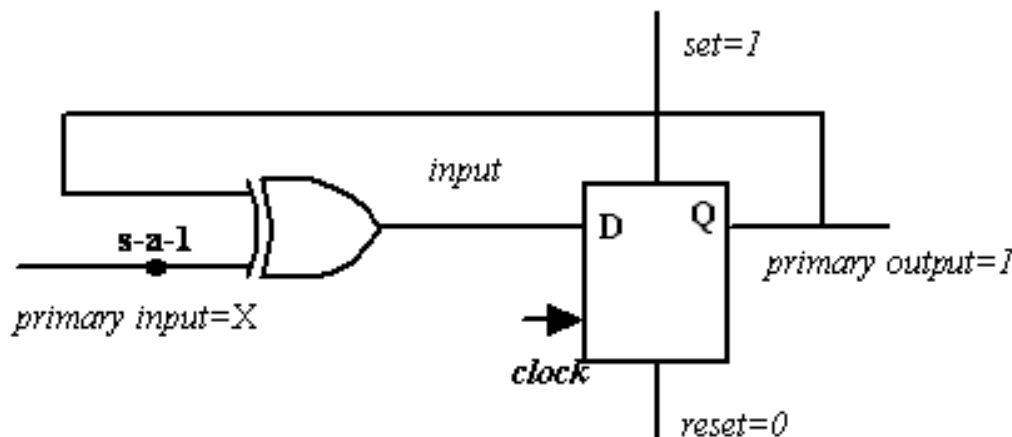
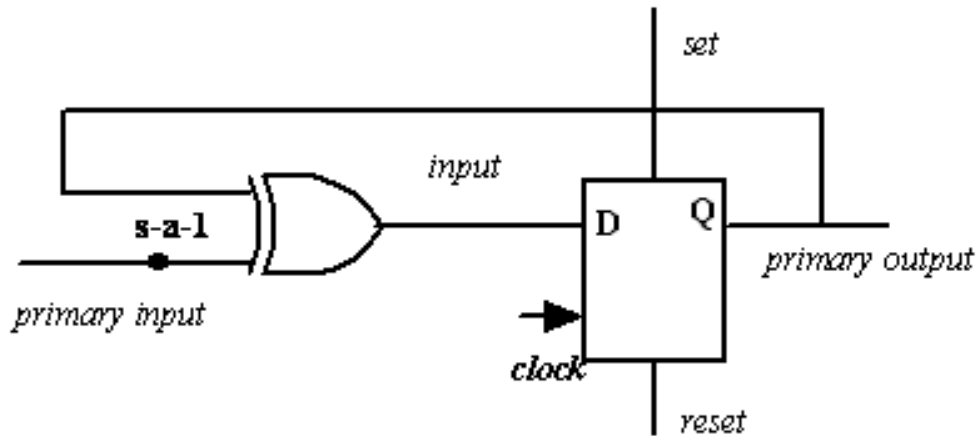
One of the simplest way to directly control flip-flops is through set-reset lines. Set-reset lines can directly make the output of a flip-flop to be 1/0 without any input and clock pulse.



Input (D)	Output (Q)	<i>set</i>	<i>reset</i>	<i>clock</i>
Don't care	1	1	0	Don't care
Don't care	0	0	1	Don't care
Don't care	Illegal	1	1	Don't care
1	1	0	0	Clock edge
0	0	0	0	Clock edge

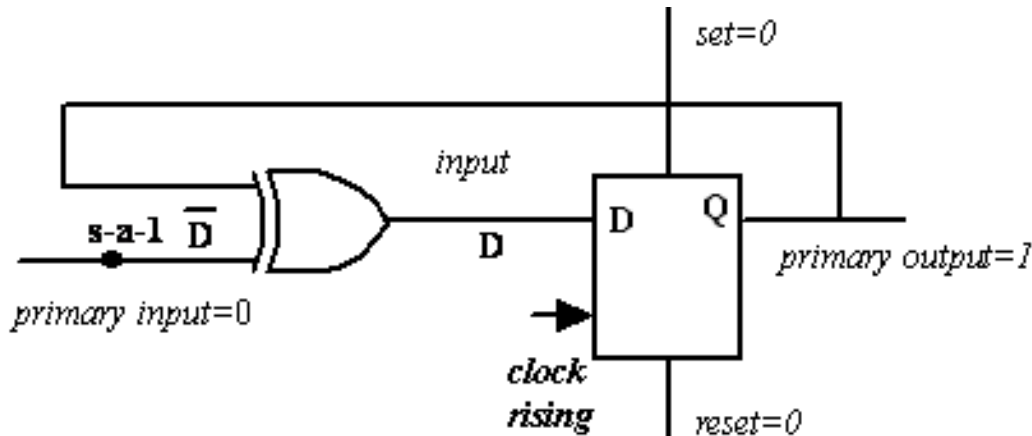
ATPG : Controllability and observability of flip-flops

- By D-algorithm, a test pattern would be: *primary input* =0, *secondary input* (other input of XOR gate)=0 and fault effect at *primary output*=D.
- So in Step-1, *set*=1 and *reset*=0 (and *primary input* =X); this makes output of flip-flop (i.e., secondary input) to be 1.

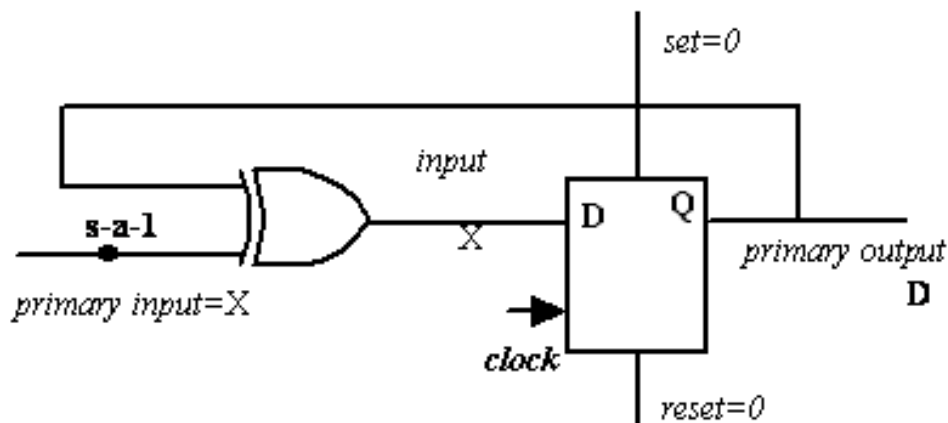


ATPG : Controllability and observability of flip-flops

- In Step-2, $set=0$, $reset=0$ and $primary\ input=0$; this sensitizes fault location as and its effect propagates to the input of the flip-flop as **D**. Also a positive clock pulse is applied which transfers **D** to output of the flip-flop (primary output).
- These two steps complete ATPG (and testing) of the fault.



**(c): Step-2: Test pattern applied
Clock pulse applied**



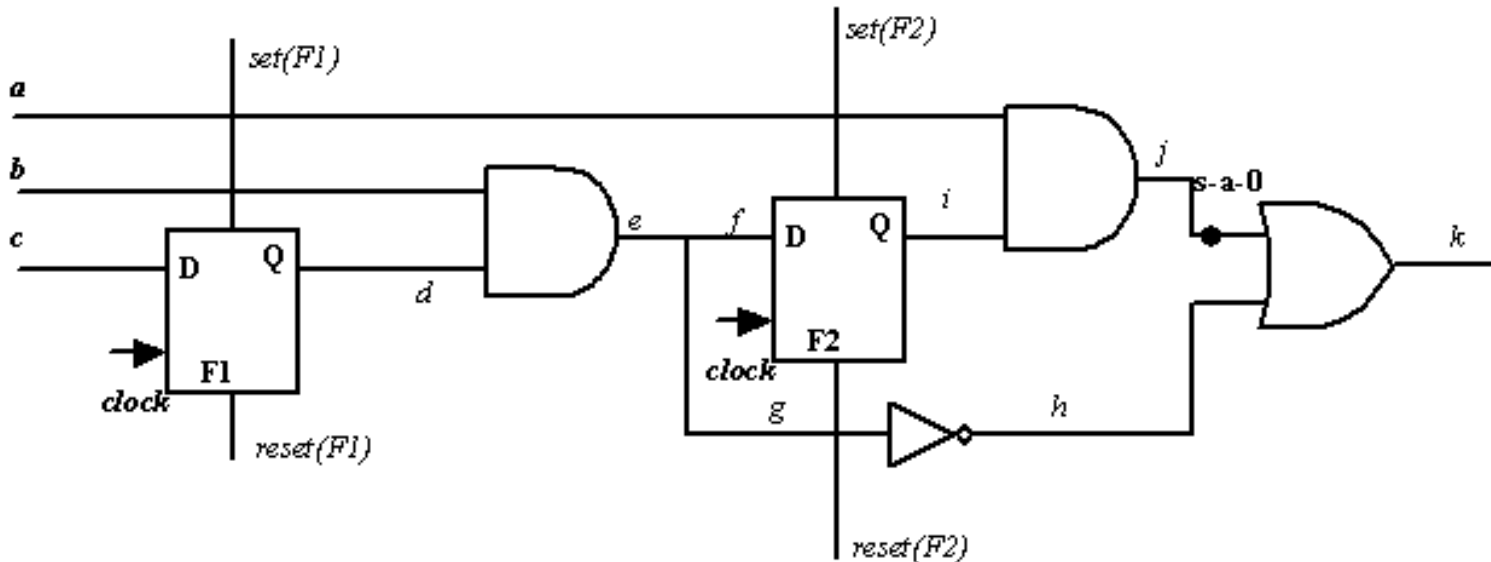
(d): Fault effect at output after clock pulse

ATPG : Controllability and observability of flip-flops

- The fault which was un-testable by time frame expansion method becomes testable using set/reset flip-flop.
- Further, one pattern is required to set/reset the flip-flops and another pattern (at primary inputs) is required to sensitize and propagate the fault effect to a primary output.
 - So, unlike time frame expansion method where $d_{seq}+1$ test patterns are required (d_{seq} patterns to initialize the flip-flops and one pattern to sensitize/propagate fault effects), in case of set/reset flip-flops only two patterns are required (one to set or reset the flops and one to sensitize/propagate fault effects).
- This saving in number of test patterns (i.e., test time)

ATPG : Controllability and observability of flip-flops

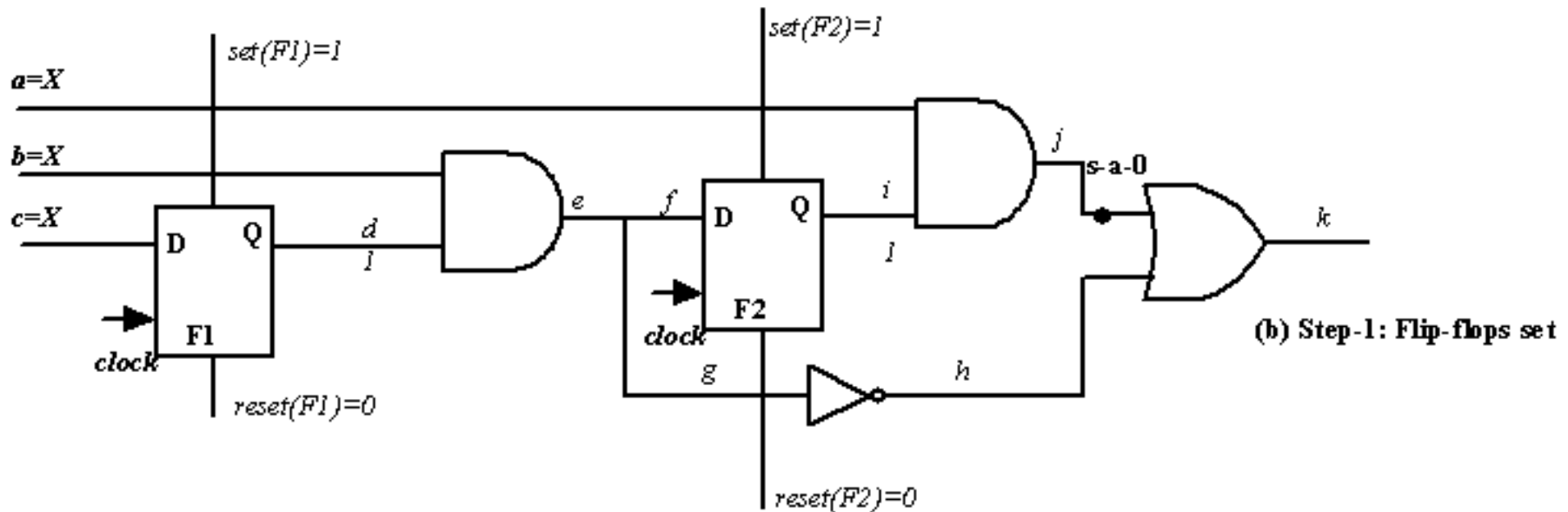
- Three patterns were required to test the s-a-0 fault at net j : (i) $a=X, b=X, c=1$ and clock pulse (ii) $a=X, b=1, c=1$ and clock pulse and (iii) $a=1, b=1, c=X$. Also it is to be noted that $d_{seq} = 2$, for the circuit.



(a) Circuit

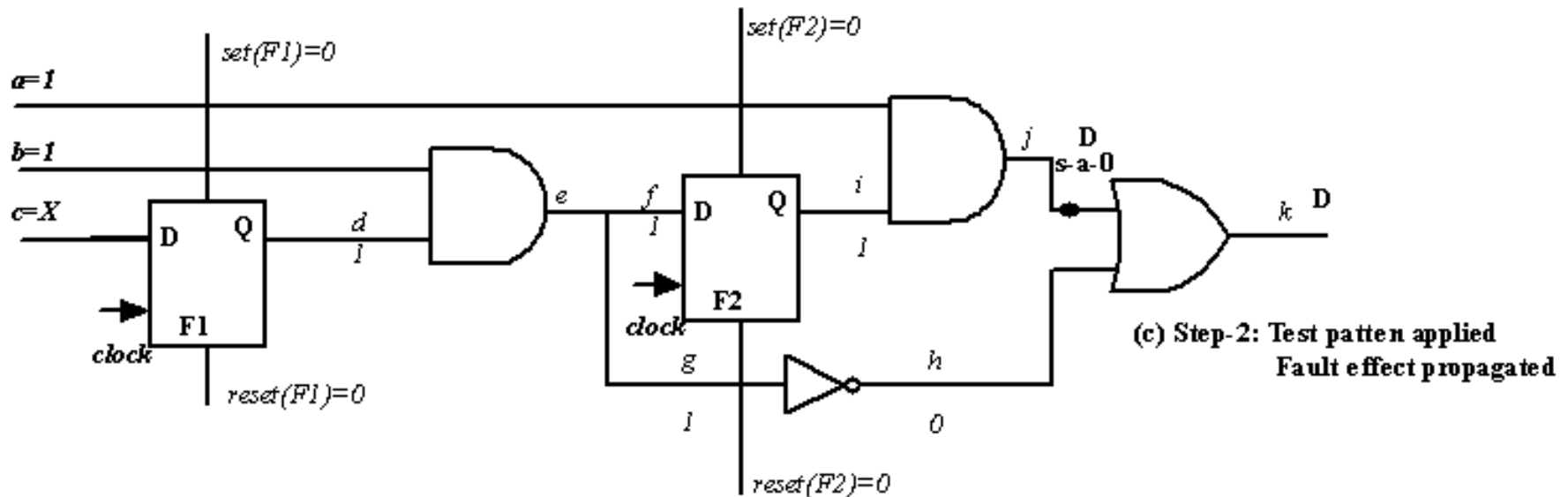
ATPG : Controllability and observability of flip-flops

- Now, by using the set/reset flip-flops, only two patterns are required to test the fault.
- By ATPG using D-algorithm, nets d and i are to be 1 for testing the fault. So both the flip-flops are set by the pattern: $a=X, b=X, c=X, set(F1)=1, reset(F1)=0, set(F2)=1$ and $reset(F2)=0$;



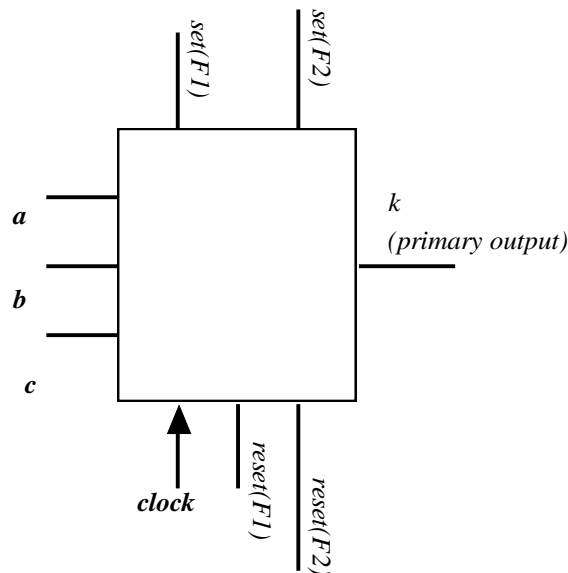
ATPG : Controllability and observability of flip-flops

- Finally, pattern $a=1, b=1, c=X$, $set(F1)=0$, $reset(F1)=0$, $set(F2)=0$ and $reset(F2)=0$ is applied to sensitize and propagate the effect of the fault to primary output.



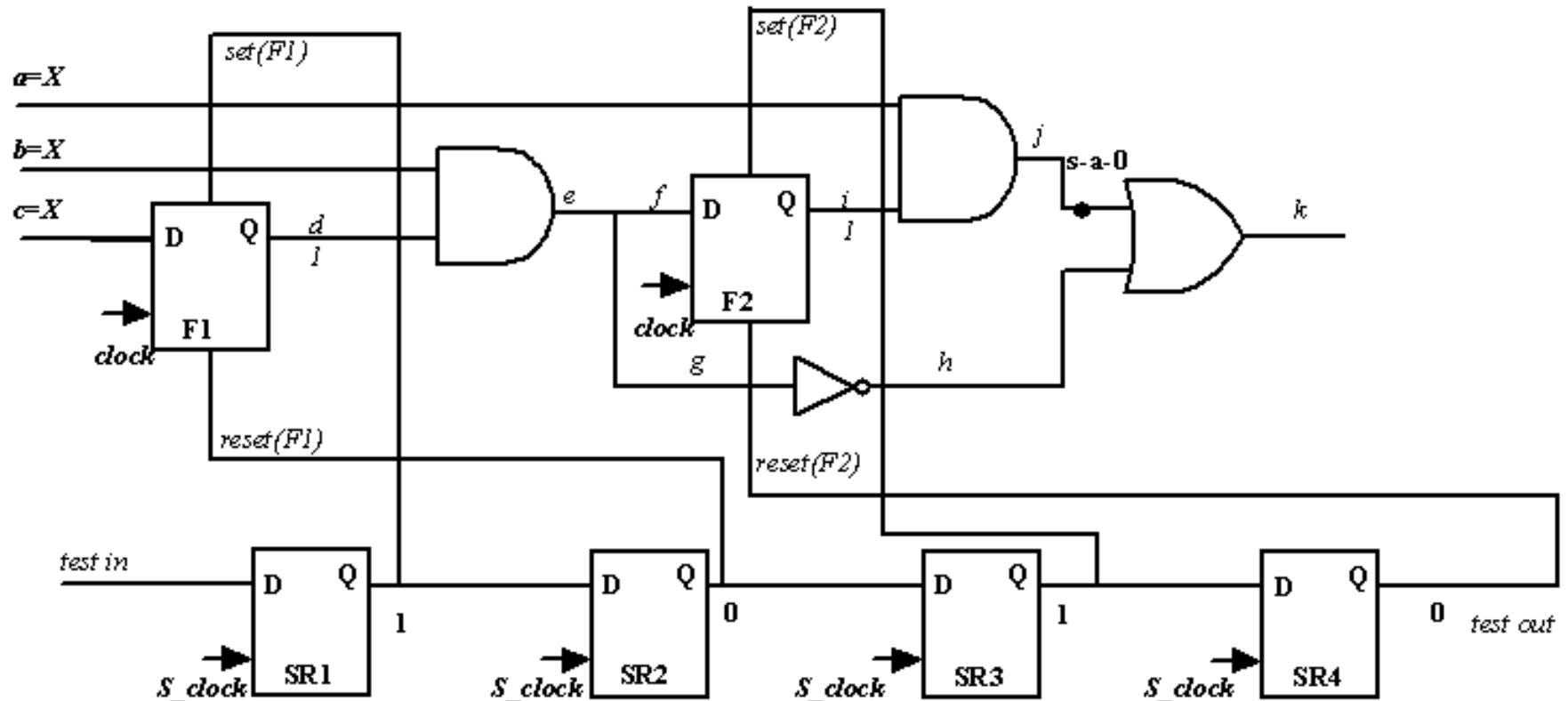
ATPG : Controllability and observability of flip-flops

- Only two patterns can test the fault.
- However the most important point is **“Irrespective of the value of d_{seq} , only two patterns are required to test a sequential circuit with set/reset flip-flops”**.
- It may be noted that it has 9 I/O pins (3 primary inputs + 1 primary output + set-reset lines, where is the number of flip-flops and a clock). The largest number of I/O pins supported in most complicated packages is about 1024. So, for a circuit with thousands of flip-flops, this approach requires a package of thousands of I/O pins (for the factor) with makes it impractical.



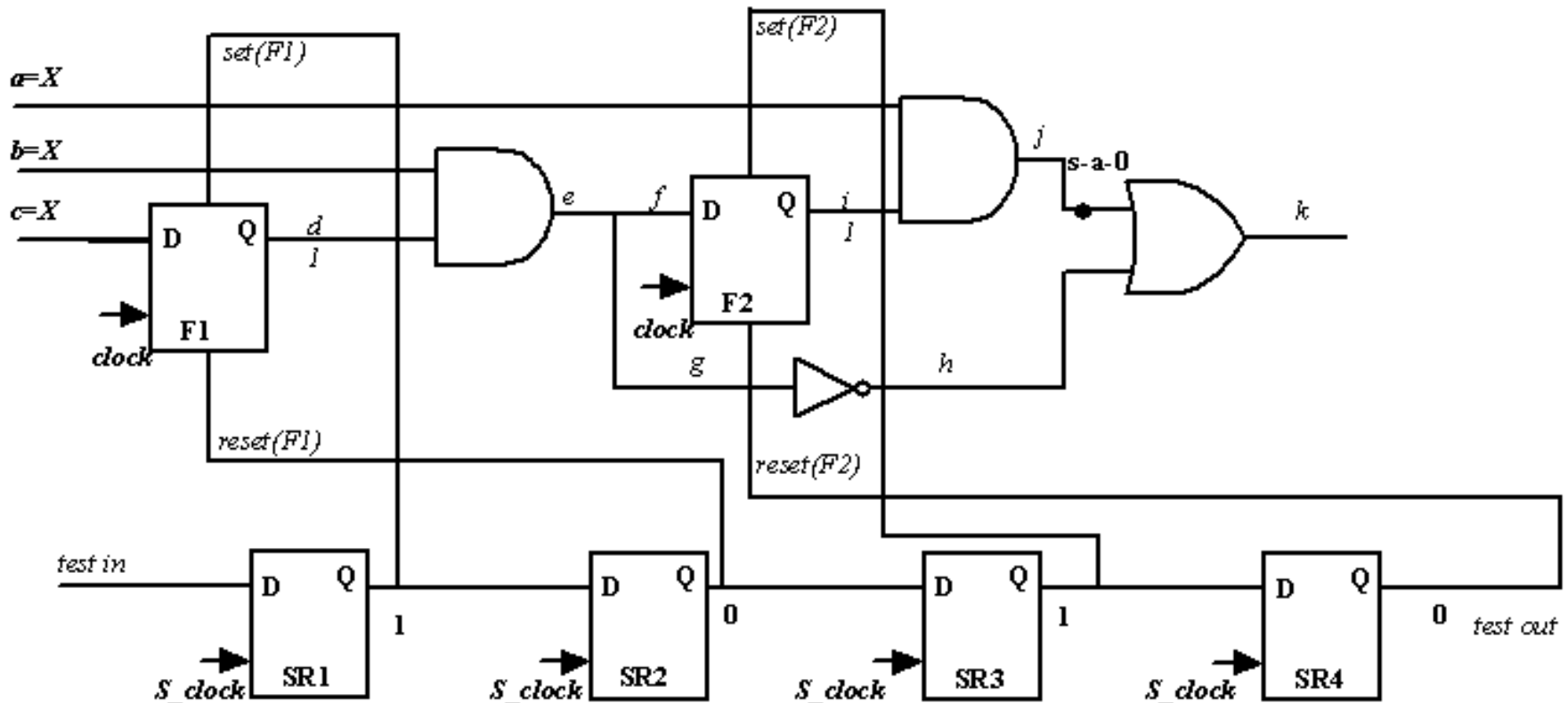
ATPG Set and reset by shift register

- To avoid this issue of high I/Os, another technique called “set and reset by shift register” is used which uses a shift register and loads itself with the pattern required for setting the flip-flops.
- In this case only three extra I/O lines are required.



ATPG Set and reset by shift register

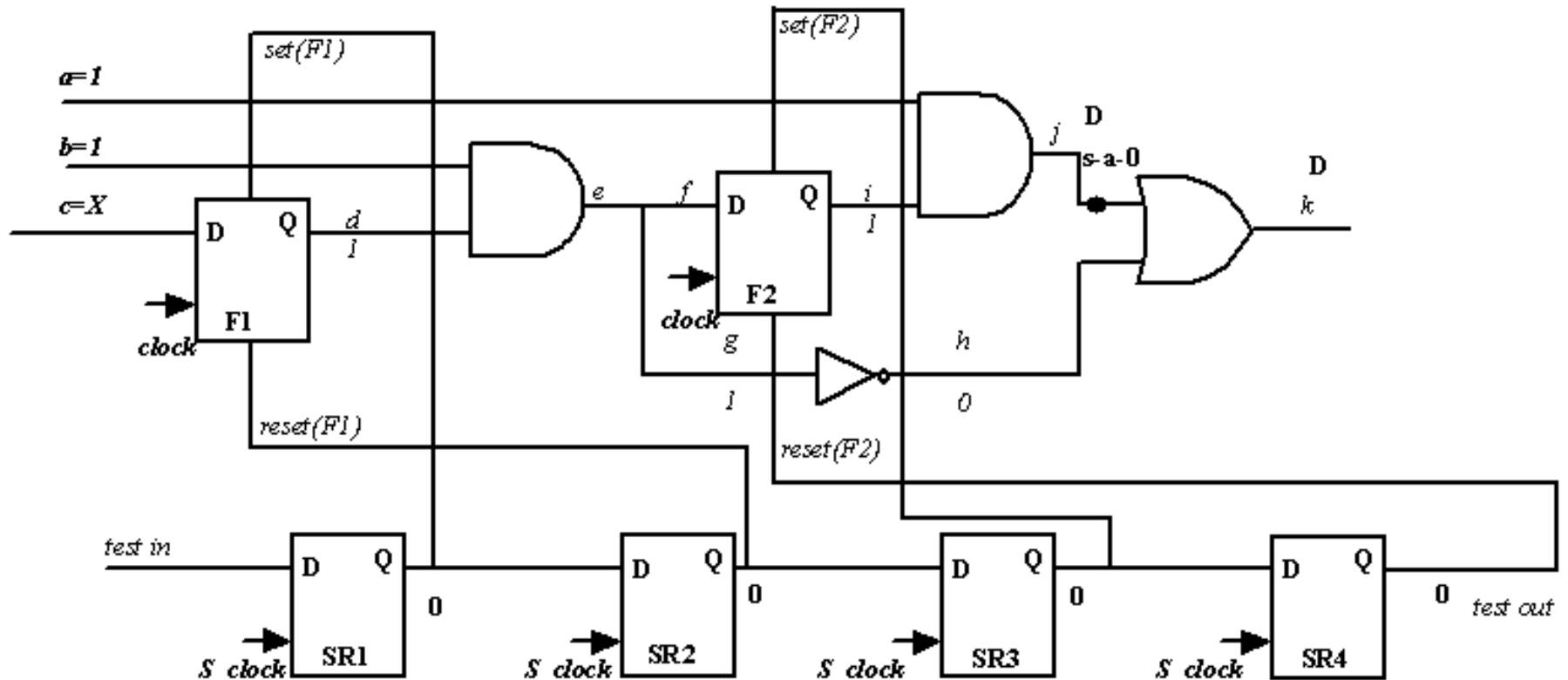
- Testing the fault (s-a-0 at j) requires the two flip-flops of the circuit to be set to
- So the pattern is $set(F1)=1, reset(F1)=0, set(F2)=1$ and $reset(F2)=0$, when mapped to the flip-flops of the shift register is $SR1=1, SR2=0, SR3=1$ and $SR4=0$.
- The pattern 1010 can be inserted in the shift register using four clock edges of S clock.



(a) Step-1: Shifting patten 1001 in the shift register
1001 in $test\ in$ @ 4 S_clock edges

ATPG Set and reset by shift register

- Now, another pattern 0000 is inserted in the shift register using four clock edges of S_clock ; this makes the circuit under test ready to be operational.
- Following that input pattern $a=1, b=1, c=X$ is applied to sensitize and propagate effect of the fault to primary output

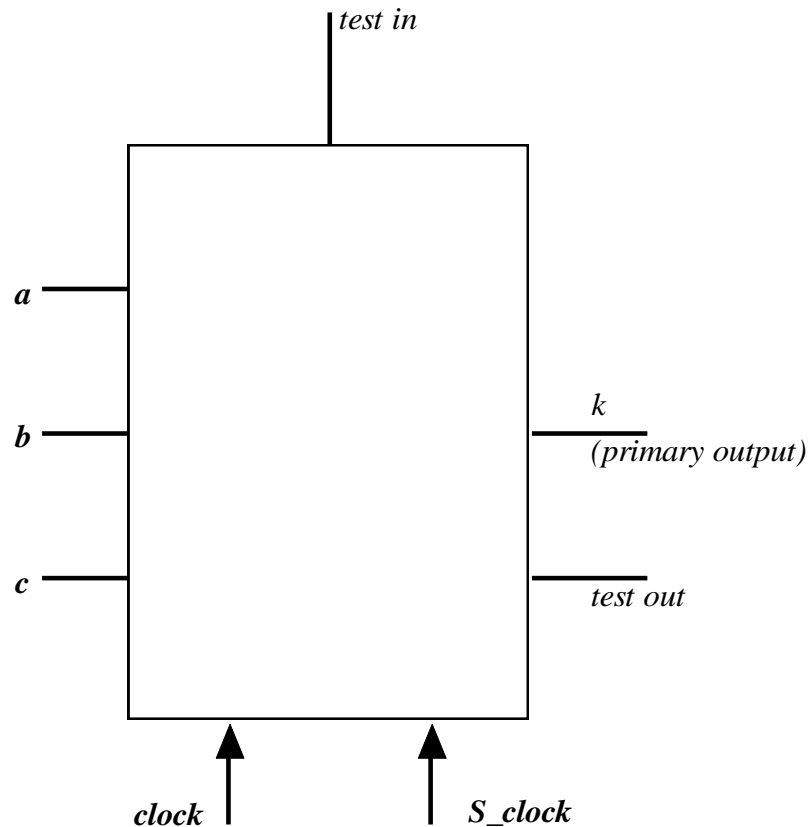


(b) Step-2: Shifting pattern 0000 in the shift register
0000 in $test\ in$ @ 4 S_clock edges

Step-3: Apply test pattern at input $a=1, b=1, c=X$

ATPG Set and reset by shift register

So in addition to original I/Os, three new I/Os get added namely, (i) *S_clock*, (ii) *test in* and (iii) *test out*.



Scan Chain based Testing and ATPG for sequential circuits

In the last section we saw that shift register based testing of sequential circuits solved the problem of a large number of I/Os. However, the major drawback of the scheme is due to the huge area overhead; twice the number of flip-flops in the circuit under test is required in the shift register.

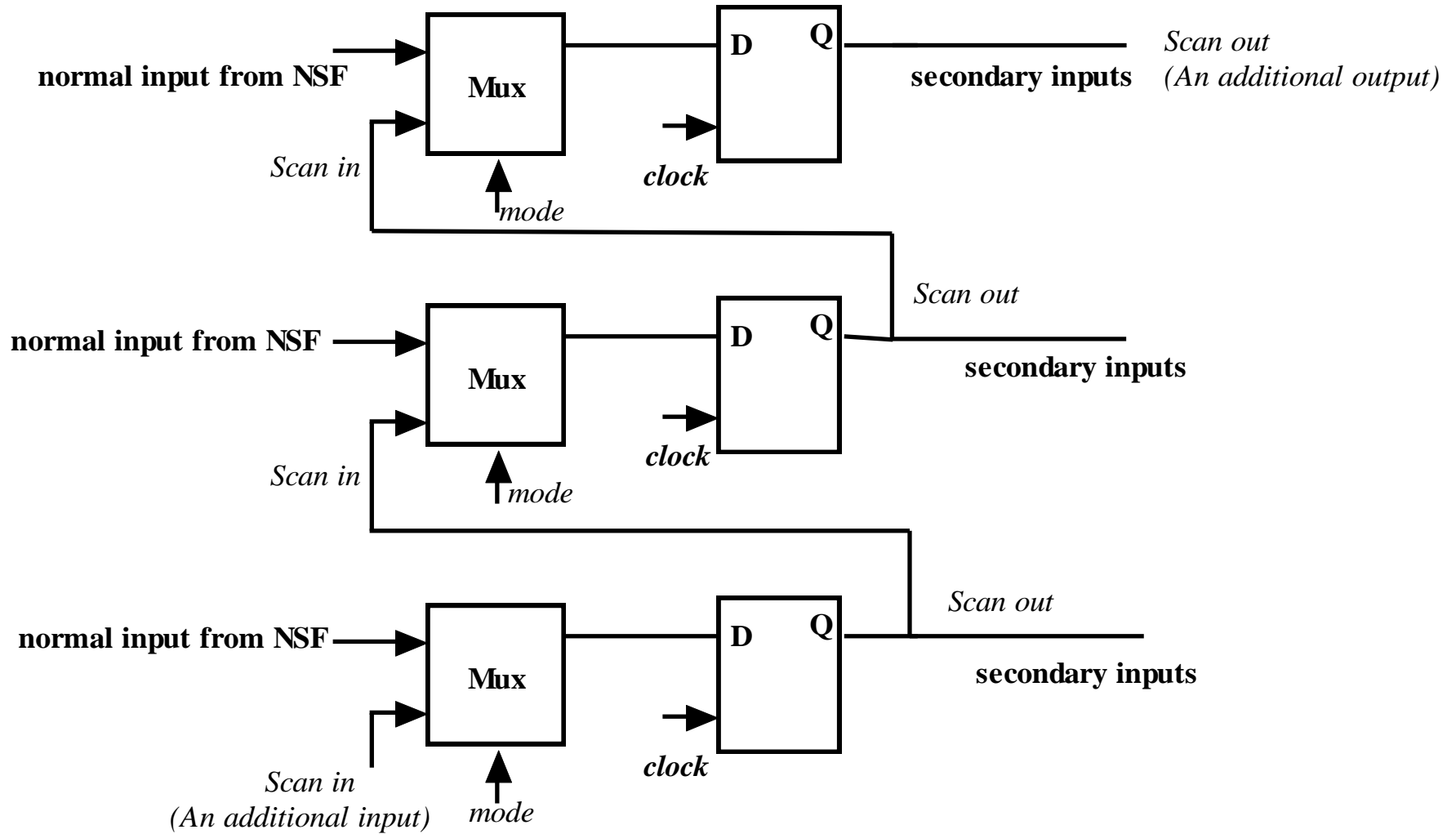
The concept of Scan chain is motivated from the idea of shift register based testing, however, alleviates the problem of area overhead. The basic idea in scan chain is to convert the flip-flops in the circuit under test itself to a shift register, rather than using a separate one.

Has two modes: (i) test (or scan chain) and (ii) working (or normal).

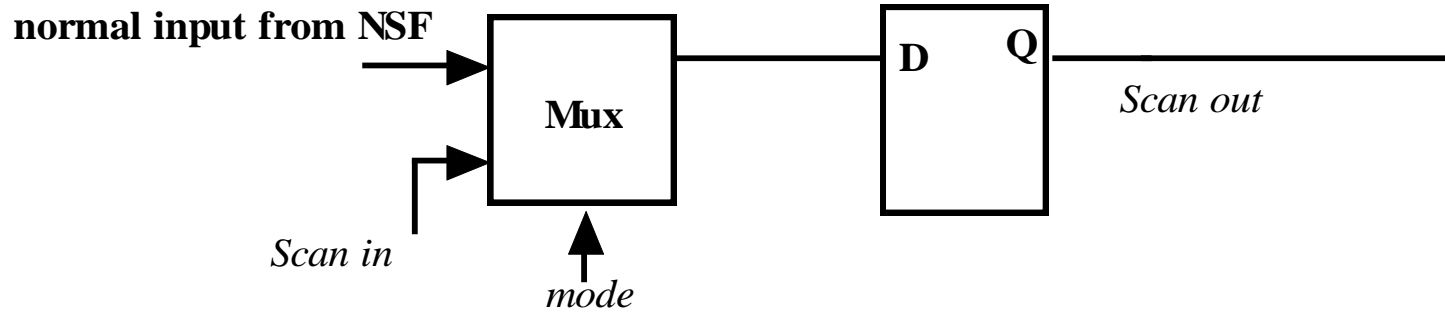
In test mode the flip-flops are decoupled from the circuit and they are connected in form of a shift register (called scan chain). Now all the flip-flops are set as required by shifting bit values in the scan chain.

Once the flip-flops are set they are removed from the scan chain and connected back to the circuit.

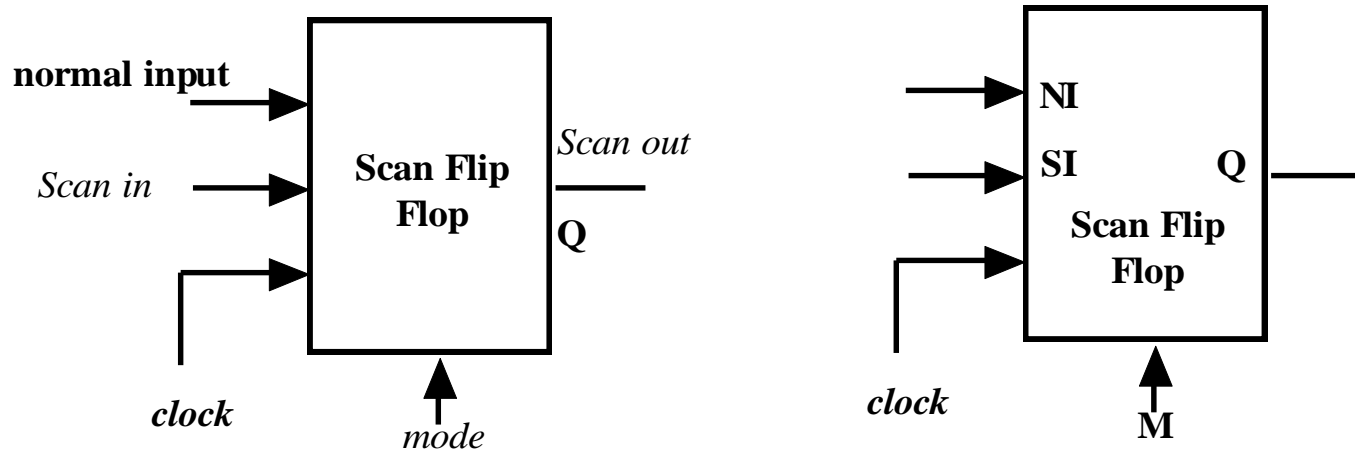
Scan Chain based Testing and ATPG for sequential circuits



Scan Chain based Testing and ATPG for sequential circuits



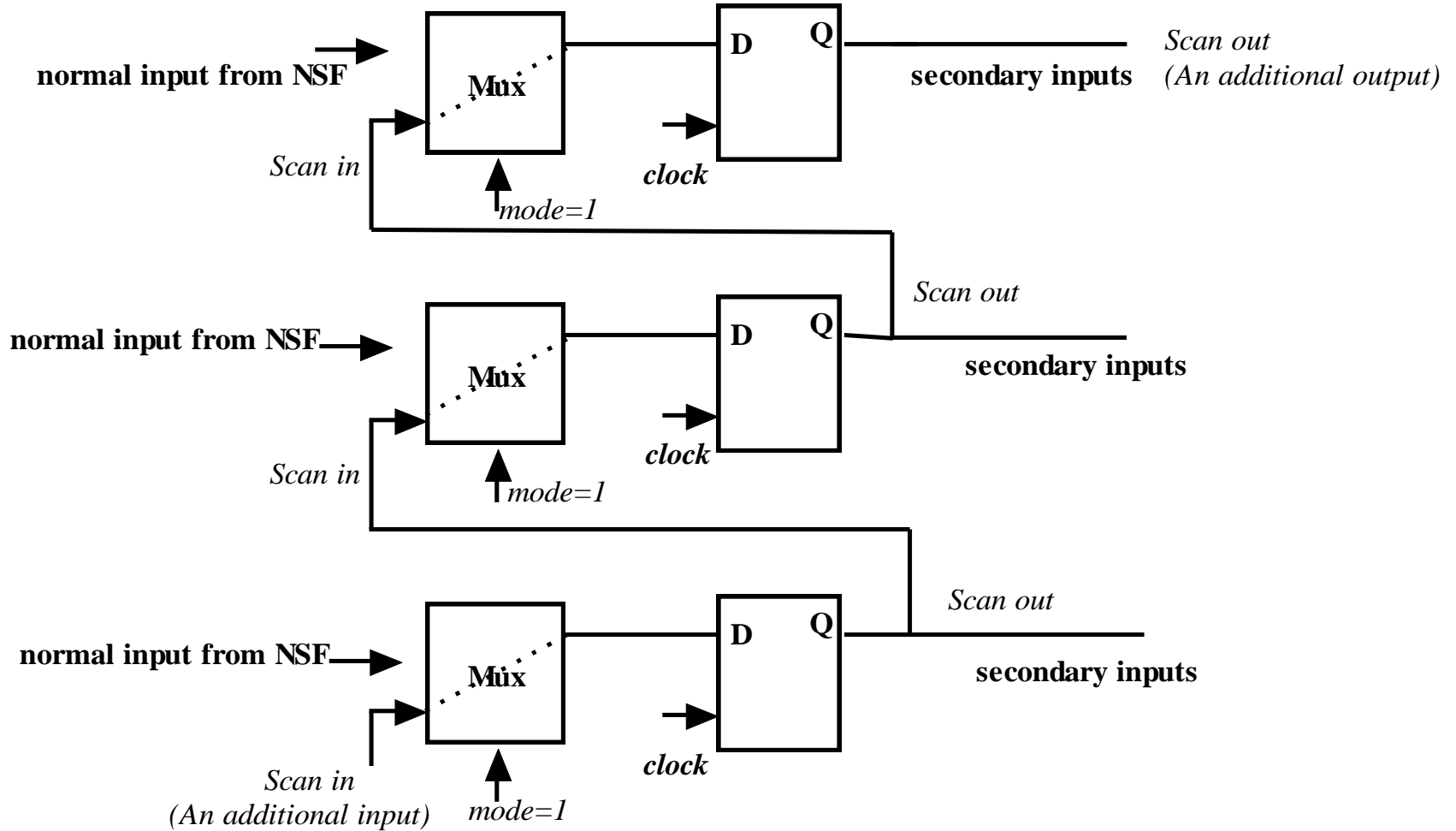
A scan flip-flop



Block diagram of a scan flip-flop

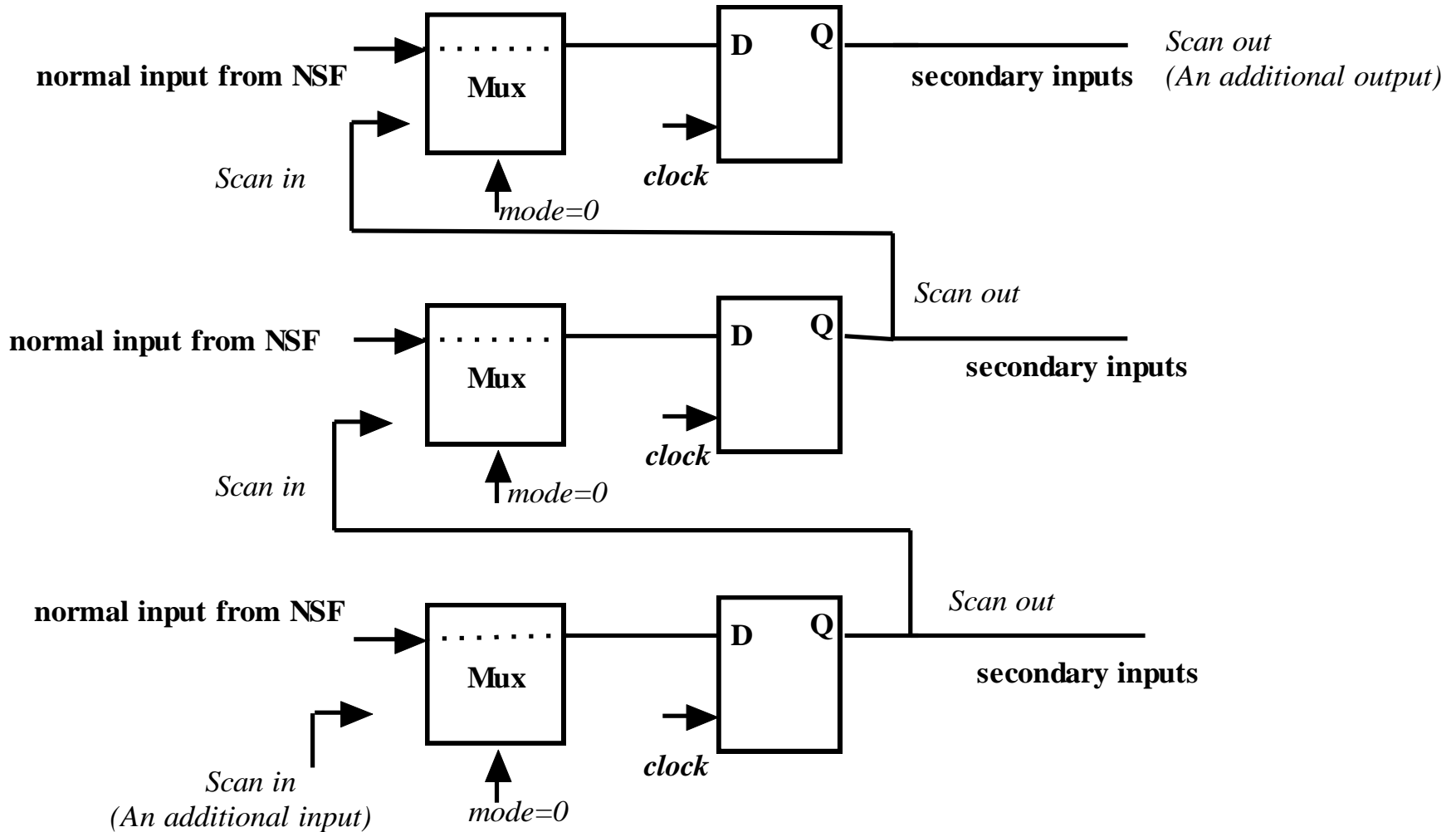
Scan Chain based Testing and ATPG for sequential circuits

Flip-flops in scan chain mode

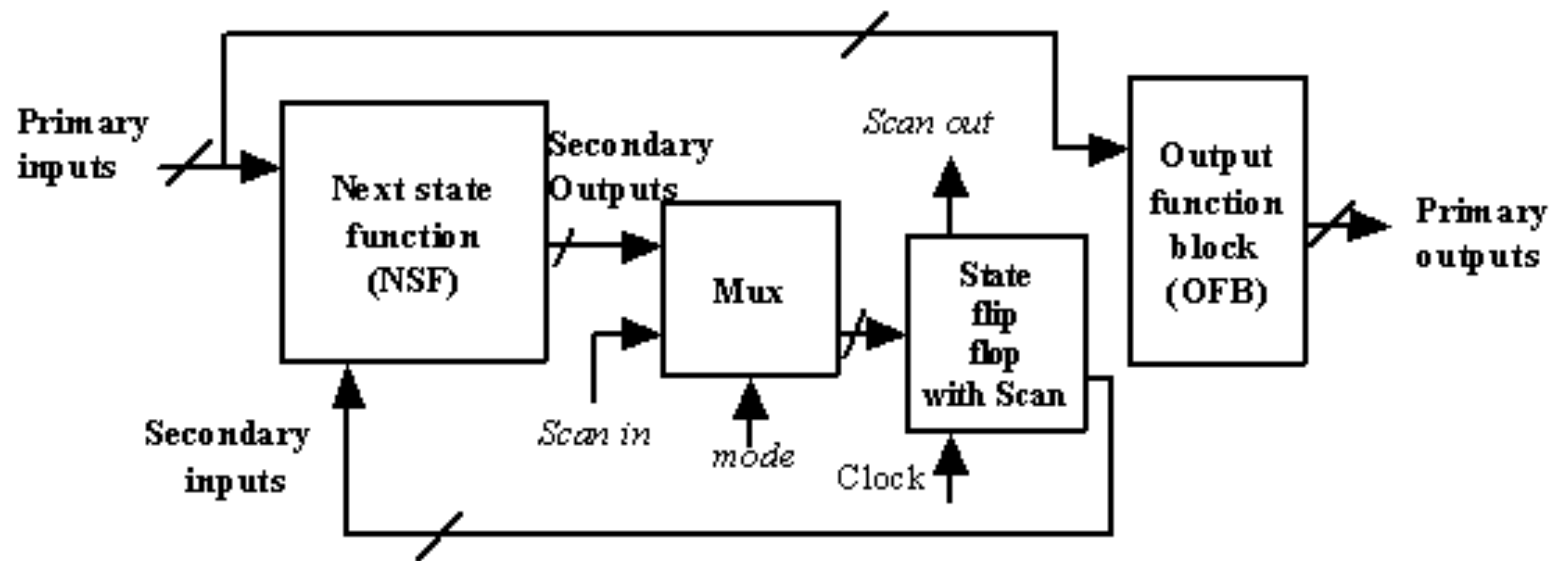


Scan Chain based Testing and ATPG for sequential circuits

Flip-flops in normal mode

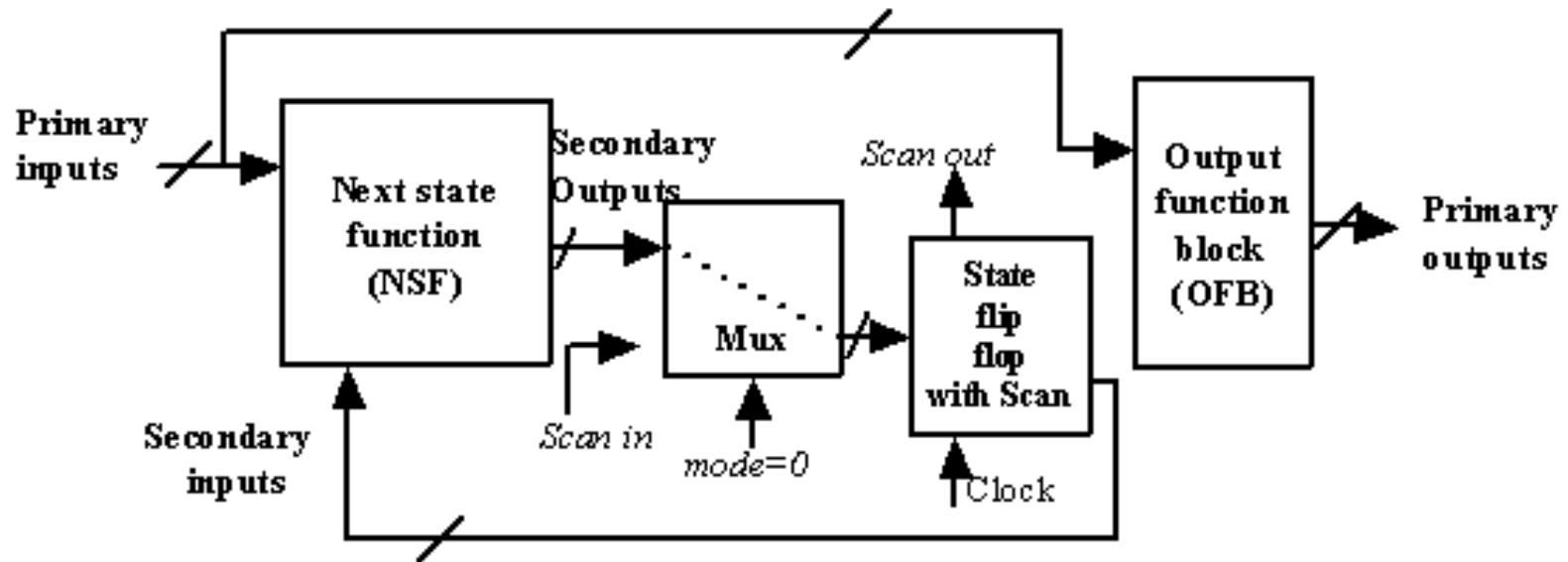


Scan Chain based Testing and ATPG for sequential circuits



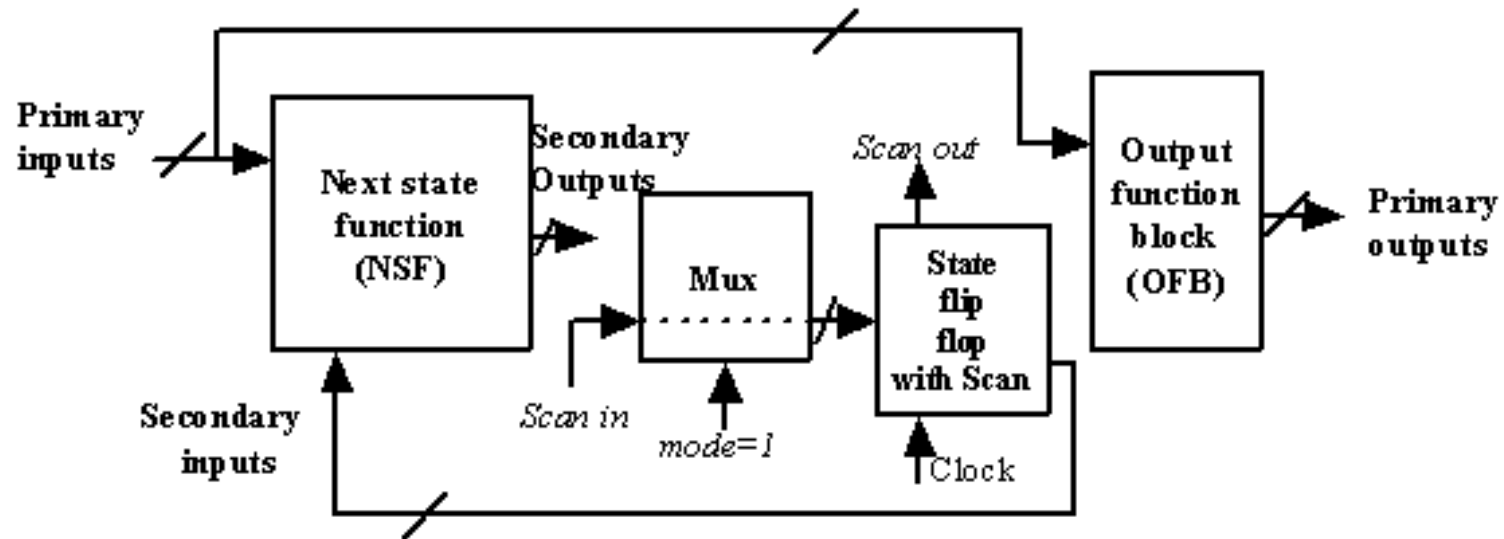
(a) Sequential Circuit with Scan Chain

Scan Chain based Testing and ATPG for sequential circuits



(b) Sequential Circuit with Scan Chain: Normal Mode

Scan Chain based Testing and ATPG for sequential circuits



(c) Sequential Circuit with Scan Chain: Test Mode

Thank You

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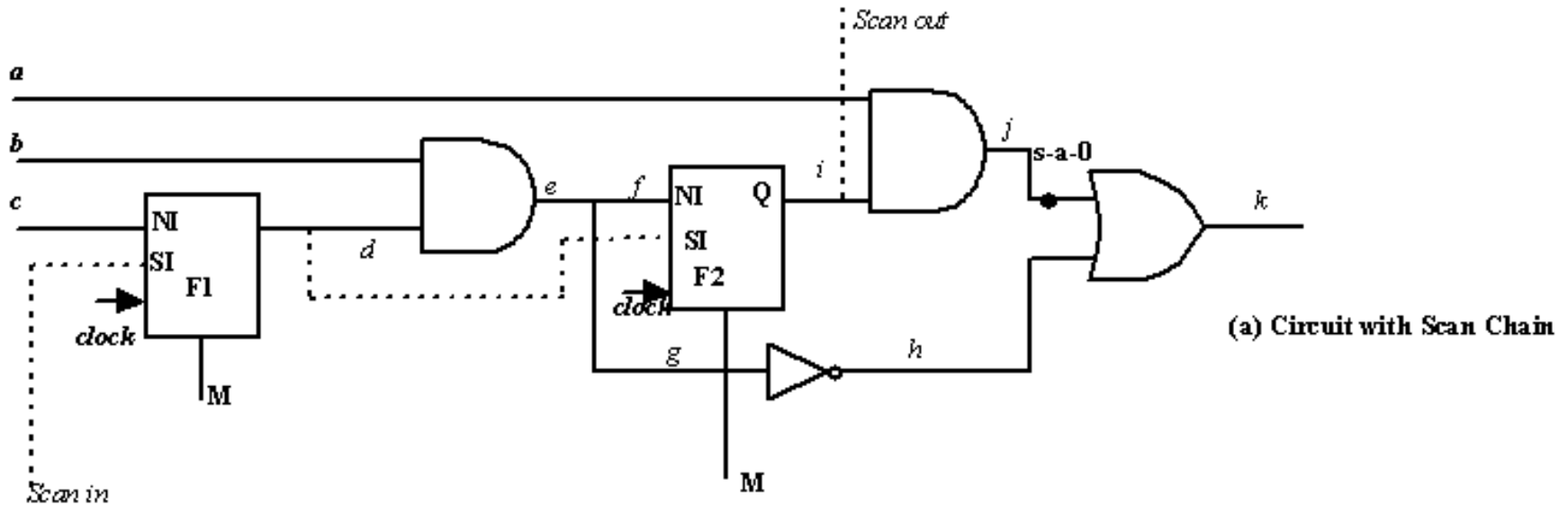
Module-X

Lecture- III

**Scan Chain based Sequential
Circuit Testing**

ATPG and testing using scan chain : An Example

The sequential circuit (running example) now with scan chain--To test the s-a-0 fault at net j , the signal values at nets d and i are to be 1.

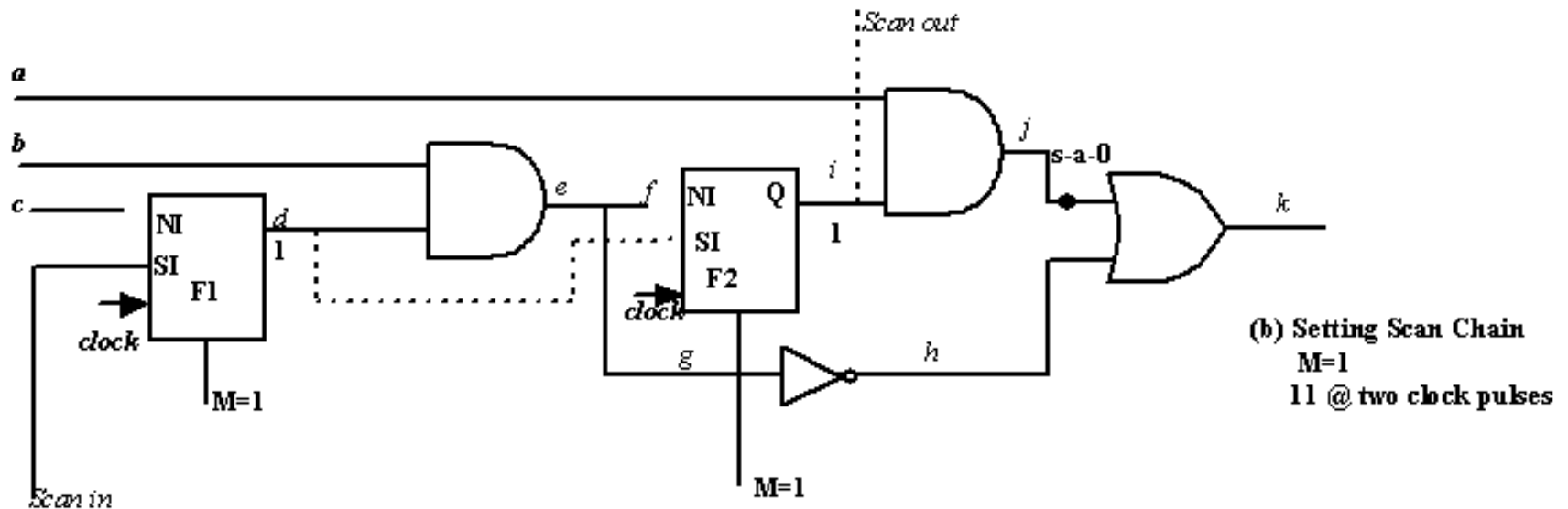


ATPG and testing using scan chain : An Example

So both the flip-flops are to be set to 1; this was achieved by making the set input as 1 and reset input as 0 in case of testing using set/reset flip-flops.

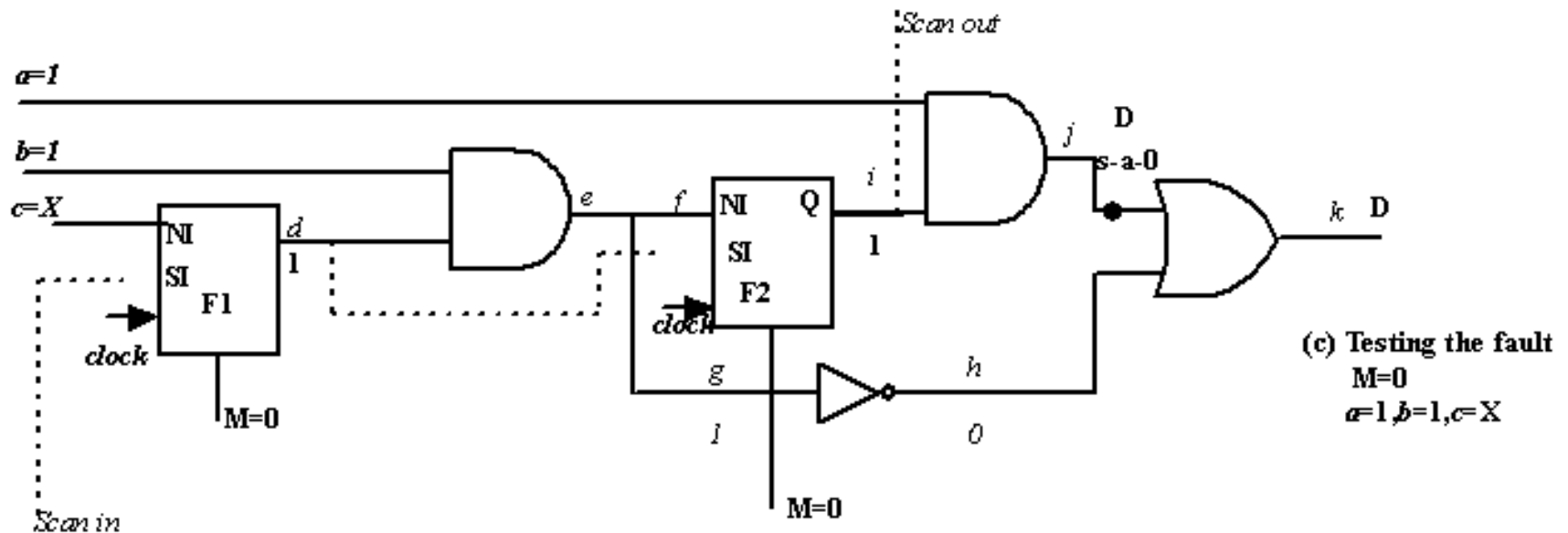
In case of scan chain, to set the flip-flops,

- Making $M=1$, removes the next state function block from the circuit and the flip-flops are connected in a chain
- Two 1s are applied in the Scan in input at two clock pulses which makes $d=1$ and $i=1$.



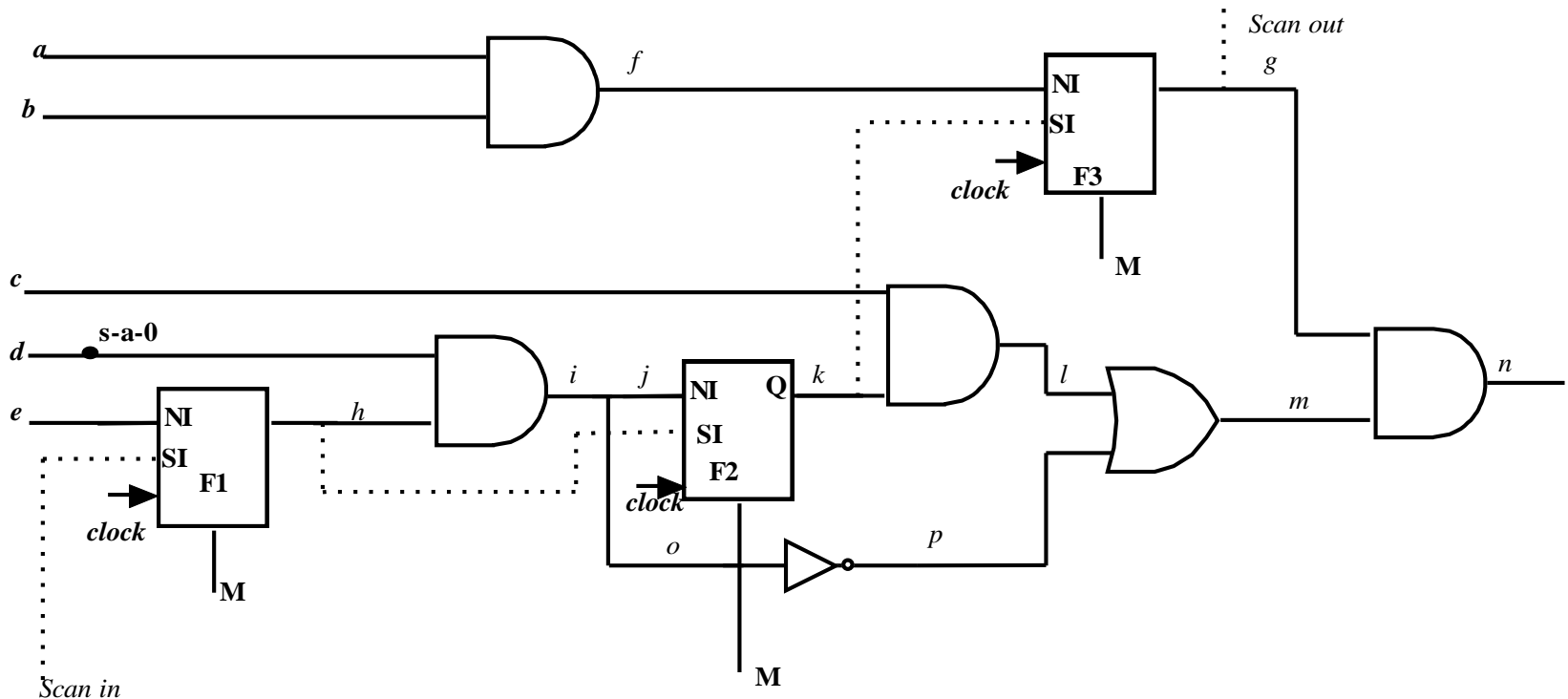
ATPG and testing using scan chain in a sequential circuit: An Example

- Circuit is brought in normal mode by making $M=0$. In this stage testing is performed by making $a=1, b=1, c=X$ which propagates the fault effect to the output



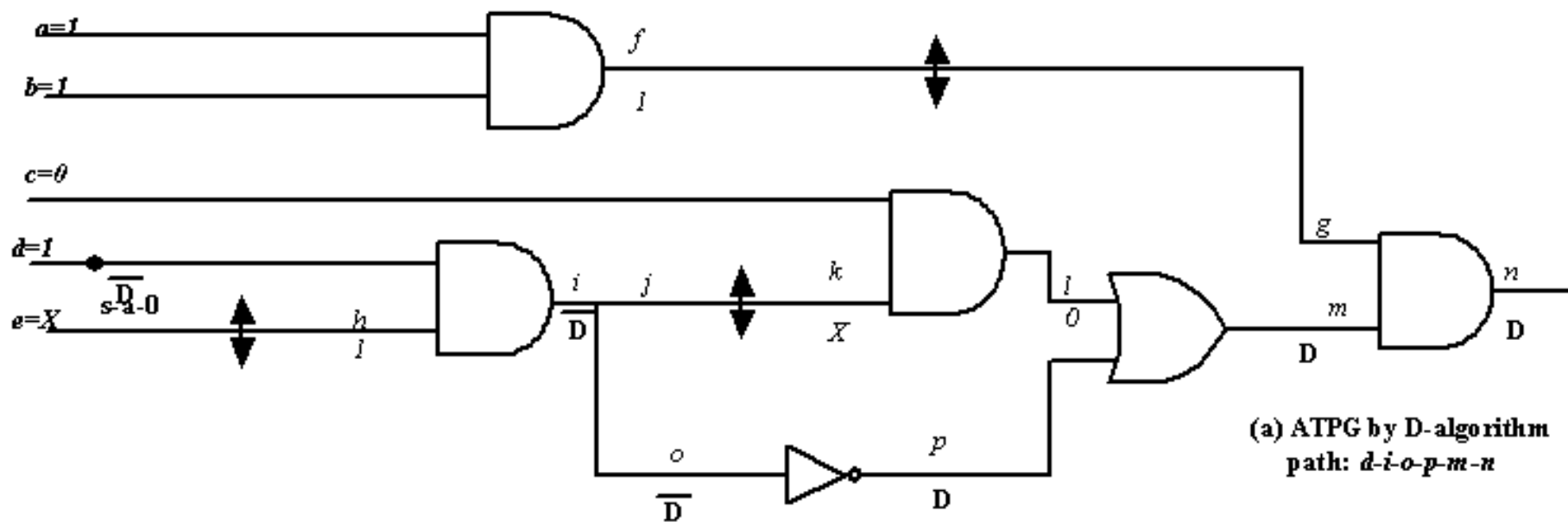
ATPG and testing using scan chain : Another Advantage

- Scan chain can be used to set the flip-flops to desired value for testing. However, D-algorithm is required on the entire circuit (after removing flip-flops) to find the test pattern.
- Eliminates the need for performing ATPG on the whole circuit.
- Consider input of the nearest flip-flop from the fault site as an output line and perform ATPG on the sub-circuit lying in the cone of influence of the output line (i.e., input of the nearest flip-flop).



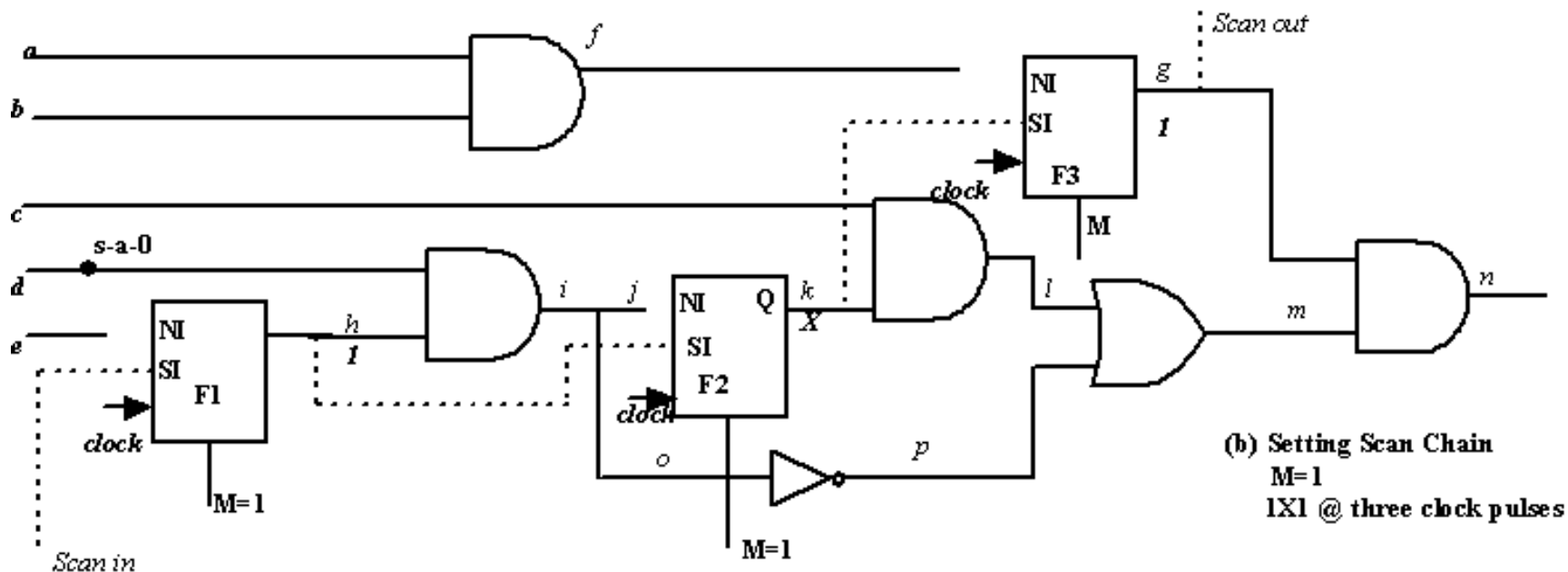
ATPG and testing using scan chain : Another Advantage

- D-algorithm applied on the full circuit (after removing the flip-flops) where fault propagation path is taken as *d-i-o-p-m-n*.
- D-algorithm determines that *h* is to be 1 and *g* is to be 1;
 - this implies that flip-flop F1 and F3 are to be set while F2 can be set or reset.



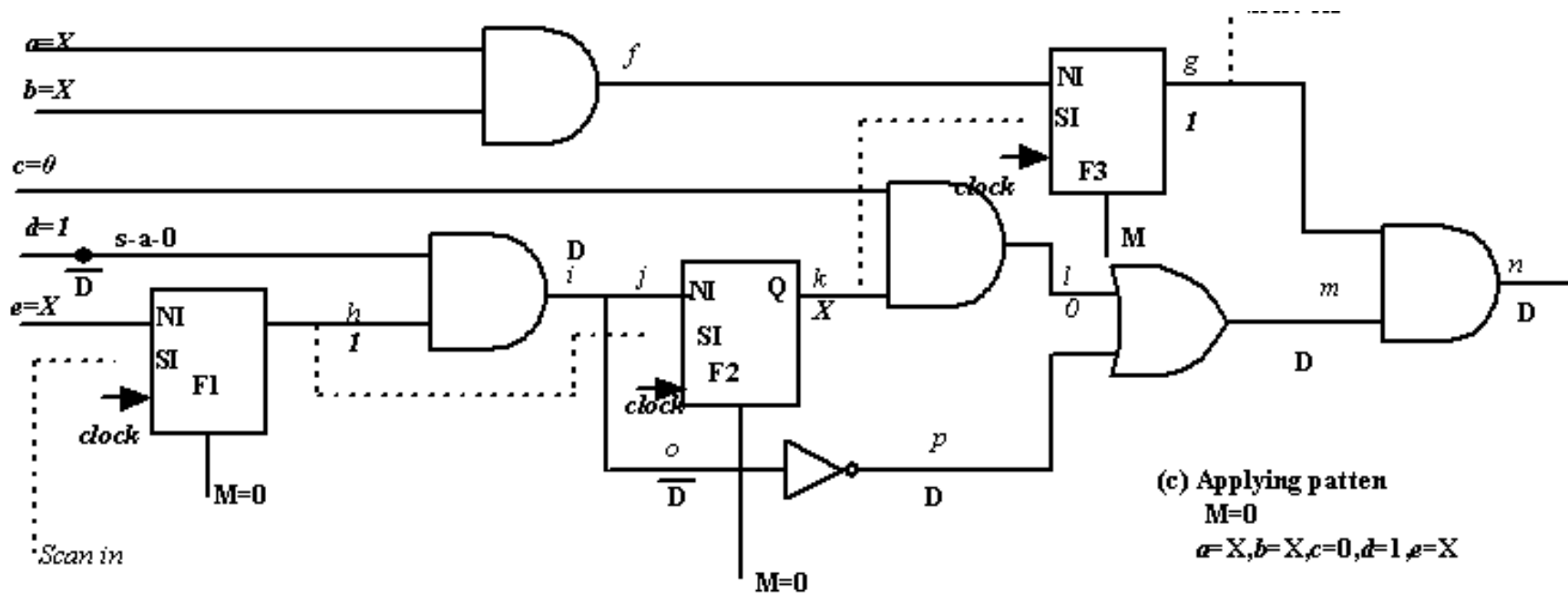
ATPG and testing using scan chain : Another Advantage

- Further, $a=X, b=X, c=0, d=1, e=X$ would apply the pattern to sensitize and propagate the fault effect.
- So to make flip-flops F1 and F3 to be 1 and F2 to be X, pattern 1X1 is applied at Scan in input with three clock pulses keeping M=1



ATPG and testing using scan chain : Another Advantage

- Finally, M is made 0 and test pattern $a=X, b=X, c=0, d=1, e=X$ is applied, which propagates fault effect through primary output n



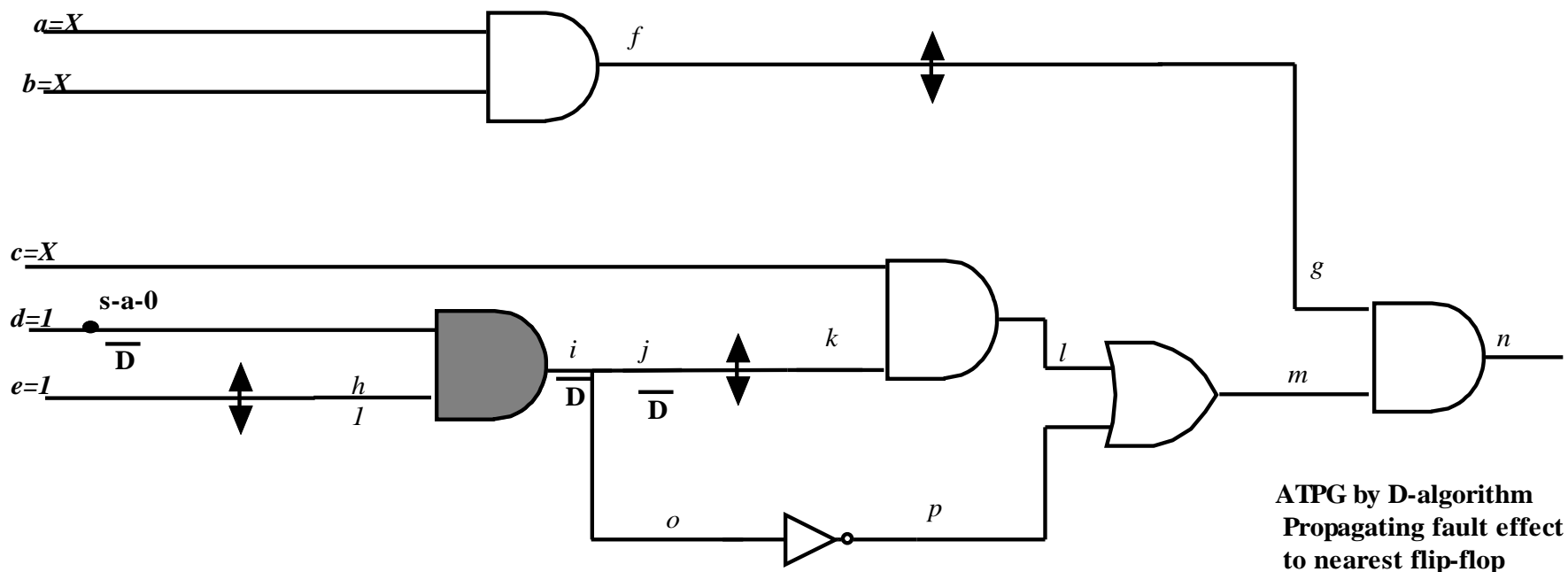
ATPG and testing using scan chain : Another Advantage

The nearest flip-flop from the fault site (s-a-0 at net d) is F2.

So fault effect needs to be propagated to net j (which is input of F2).

So, ATPG is to be performed on the sub-circuit which lies in the cone of influence of net j , which includes inputs d, e and AND gate marked gray

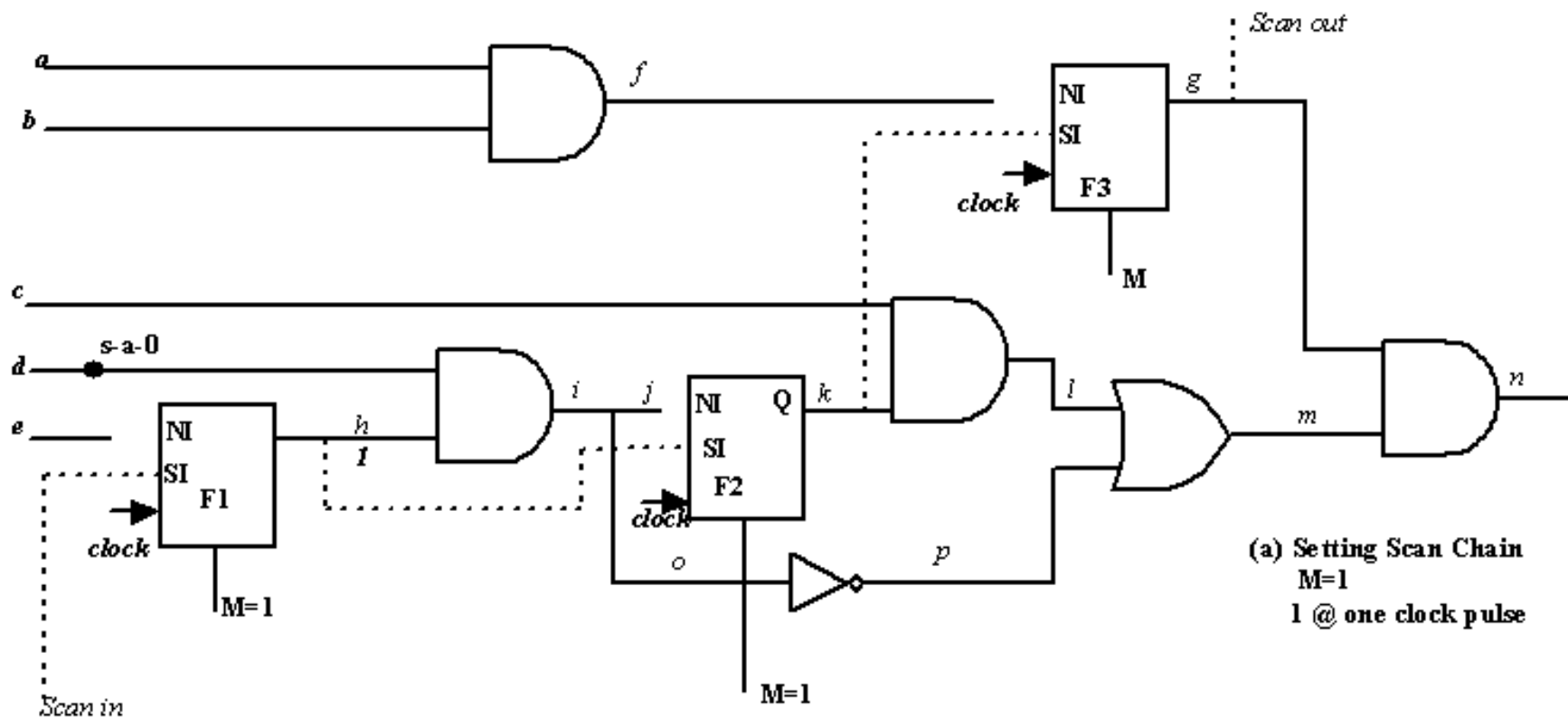
test pattern is $d=1, e=1$ and fault effect \bar{D} is propagated to net j . Obviously ATPG complexity is simplified.



ATPG and testing using scan chain : Another Advantage

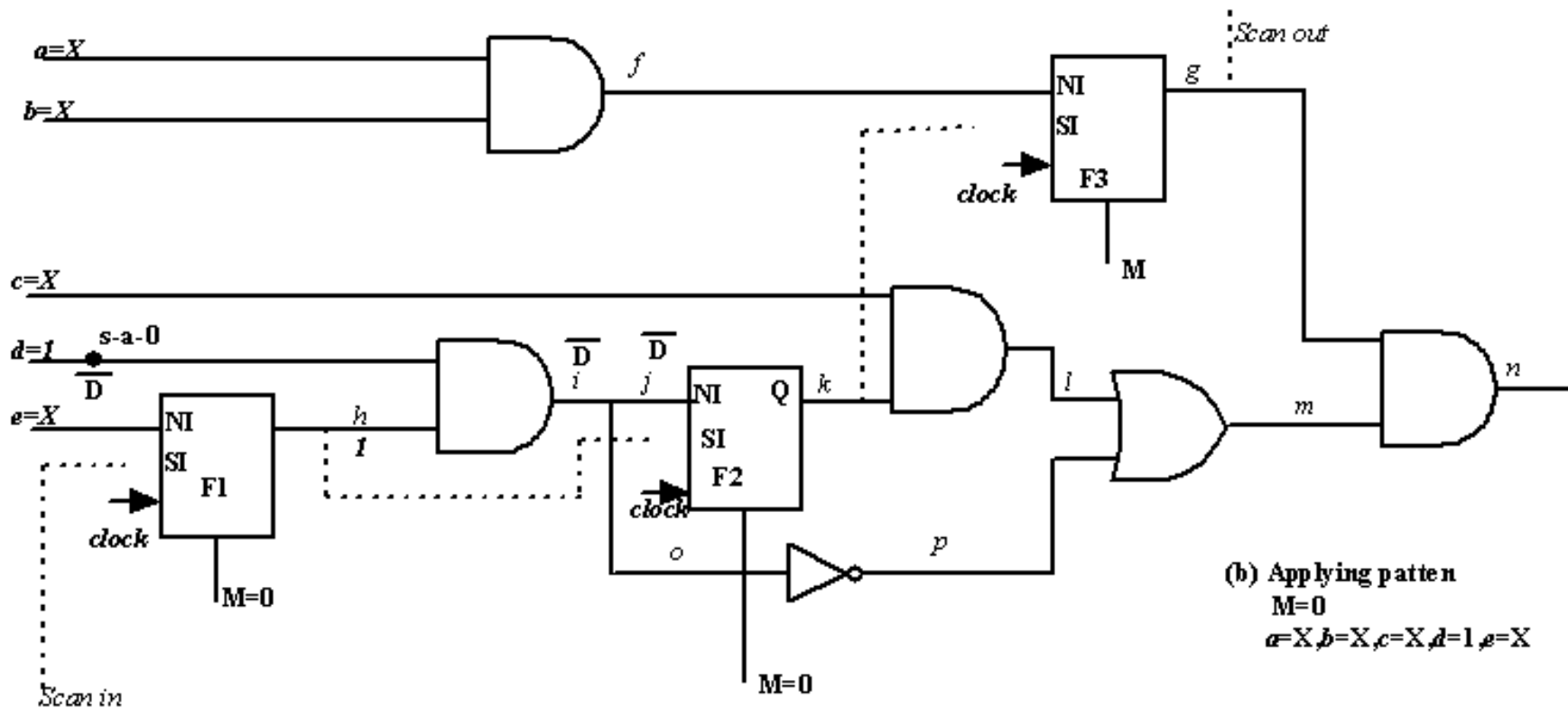
In this case, as we are considering only a sub-circuit, so only F1 (i.e., net h) needs to be made 1

This is achieved by making $M=1$, giving 1 in Scan in input and a clock pulse



ATPG and testing using scan chain : Another Advantage

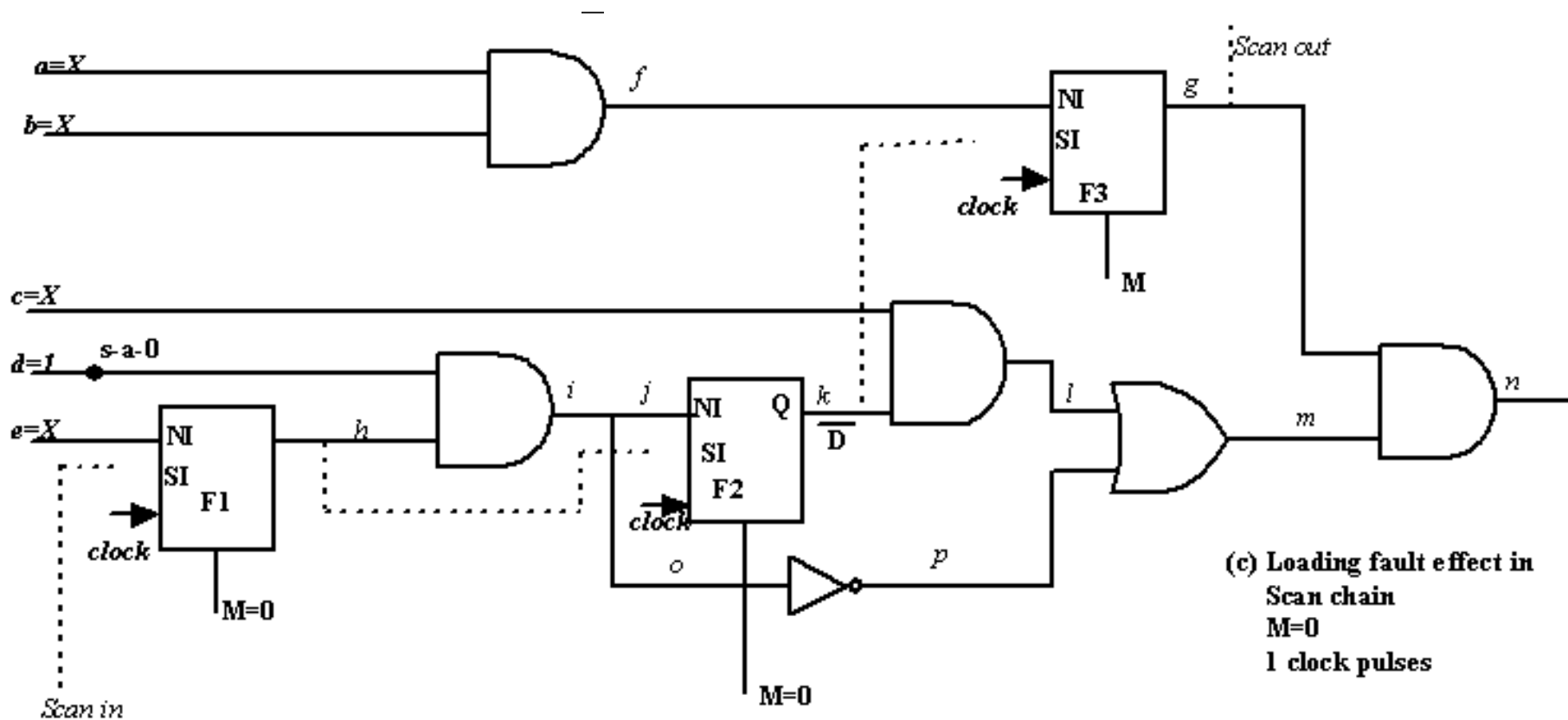
After that M is made 0 and pattern $d=1, e=X$ is applied to sensitize the fault and propagate the effect (\bar{D}) to net j via net i



ATPG and testing using scan chain : Another Advantage

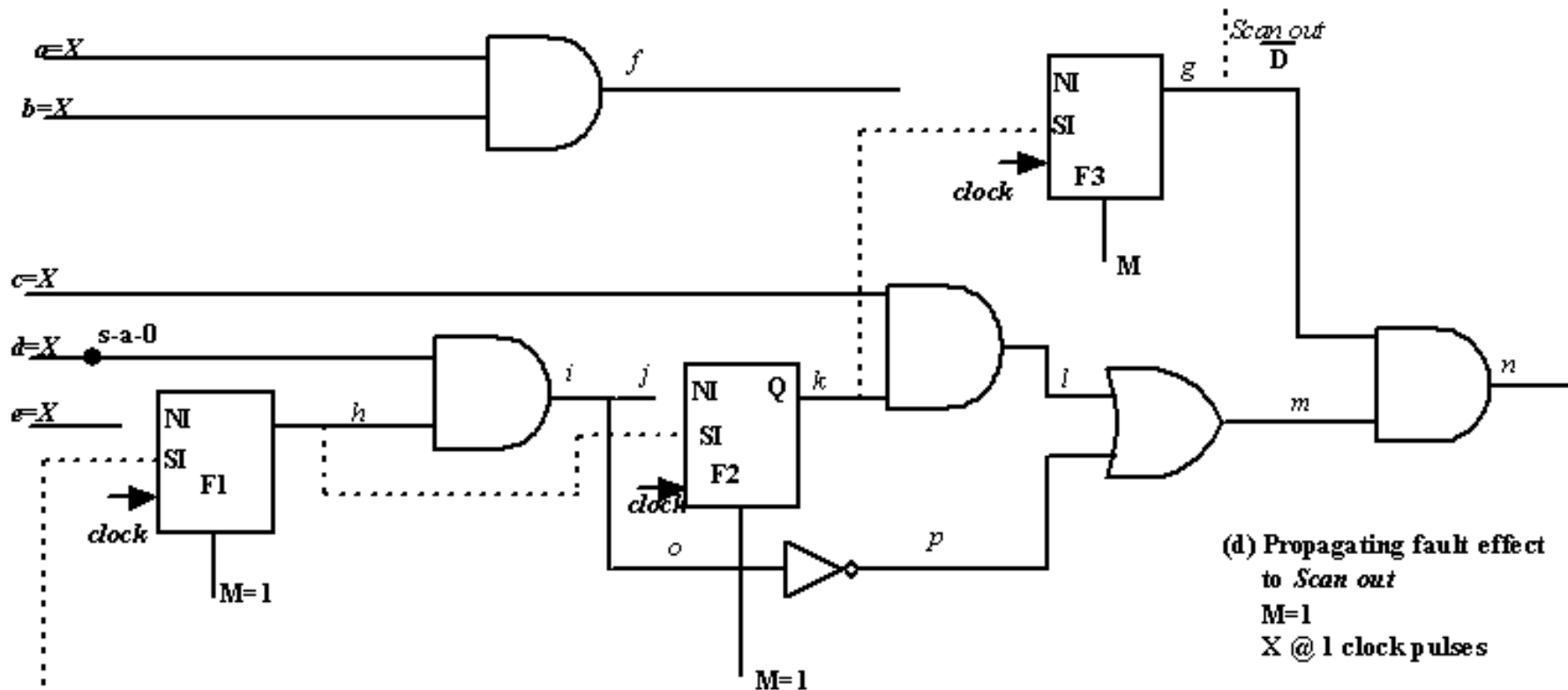
Now the fault effect is to be brought out by the scan chain.

First, the effect is loaded into the nearest flip-flop (F2) by applying a clock pulse keeping M=0



ATPG and testing using scan chain : Another Advantage

Following that flip-flops are again brought into chain mode (by setting $M=1$) and 1 clock pulse is applied (with Scan in input as X), which brings the effect out through the Scan out output

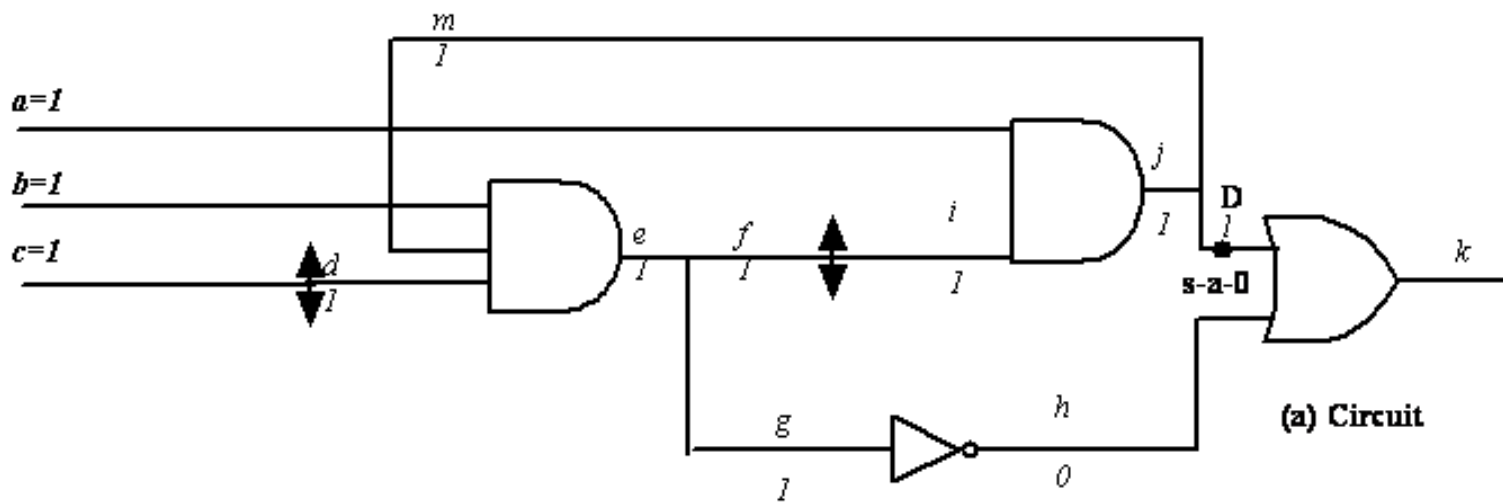


ATPG and testing using partial scan chain in a sequential circuit

- A circuit with sequential depth d_{seq} needs d_{seq} clock pulses and patterns to set the flip-flops (to required values) when testing is done using time frame expansion approach.
- In case of scan chain if there are n_{ff} flip-flops, then n_{ff} clock pulses are required to set/reset the flip-flops.
- As $n_{ff} > d_{seq}$, test time is higher for scan chain based testing compared to time frame expansion method. Also, multiplexers are required in case of scan chains while no extra circuitry is required for time frame expansion method. Only ATPG complexity is lower in case of scan based testing. It may be noted that ATPG is off line exercise and test time is very expensive as patterns are applied by an automatic test equipment.
- However, scan based testing is still the most widely accepted technology.
 - Time frame expansion scheme cannot set/reset flip-flops which are cyclic (i.e., whose input is dependent on its own output). So scan based scheme or set/reset with shift register scheme is required for cyclic circuits.

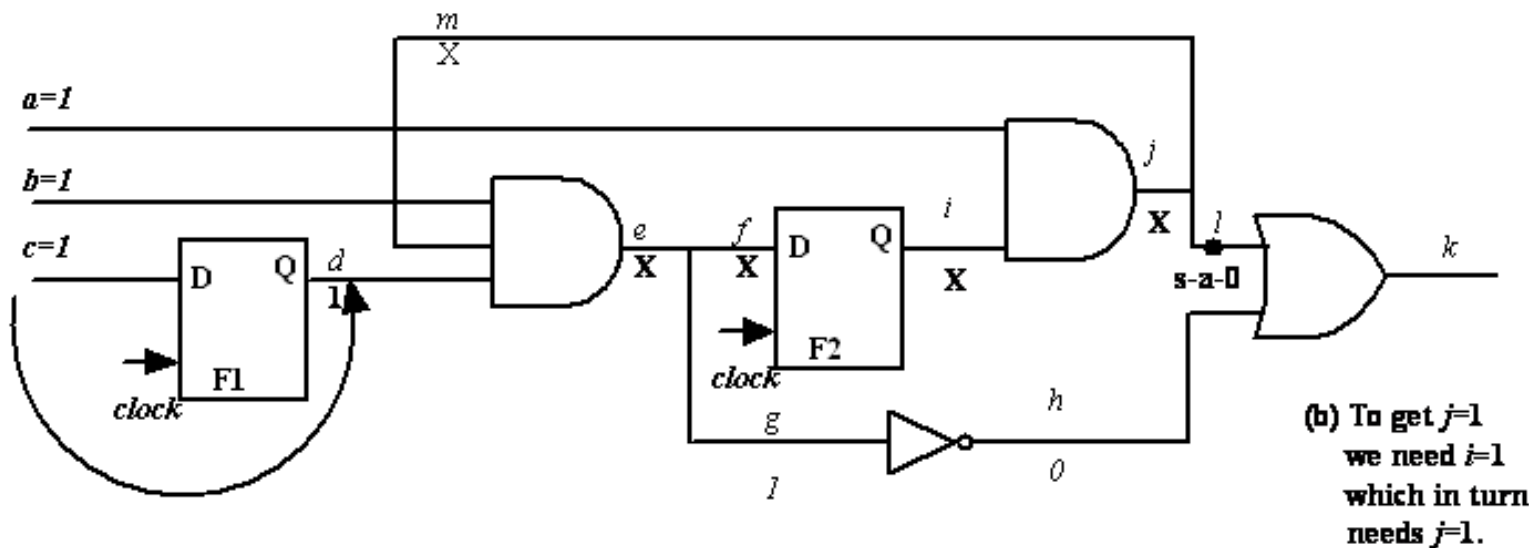
ATPG and testing using partial scan chain in a sequential circuit: An Example

- “Partial scan”--taking ideas from both time frame expansion method and scan chain method.
- The basic idea used in the scheme is to make scan enable only in those flip-flops which are cyclic and keep the remaining ones as normal.
- So we will have area overhead (because of MUX) only for those flip-flops which must be controlled directly and for the others, time frame expansion based indirect control can be used.



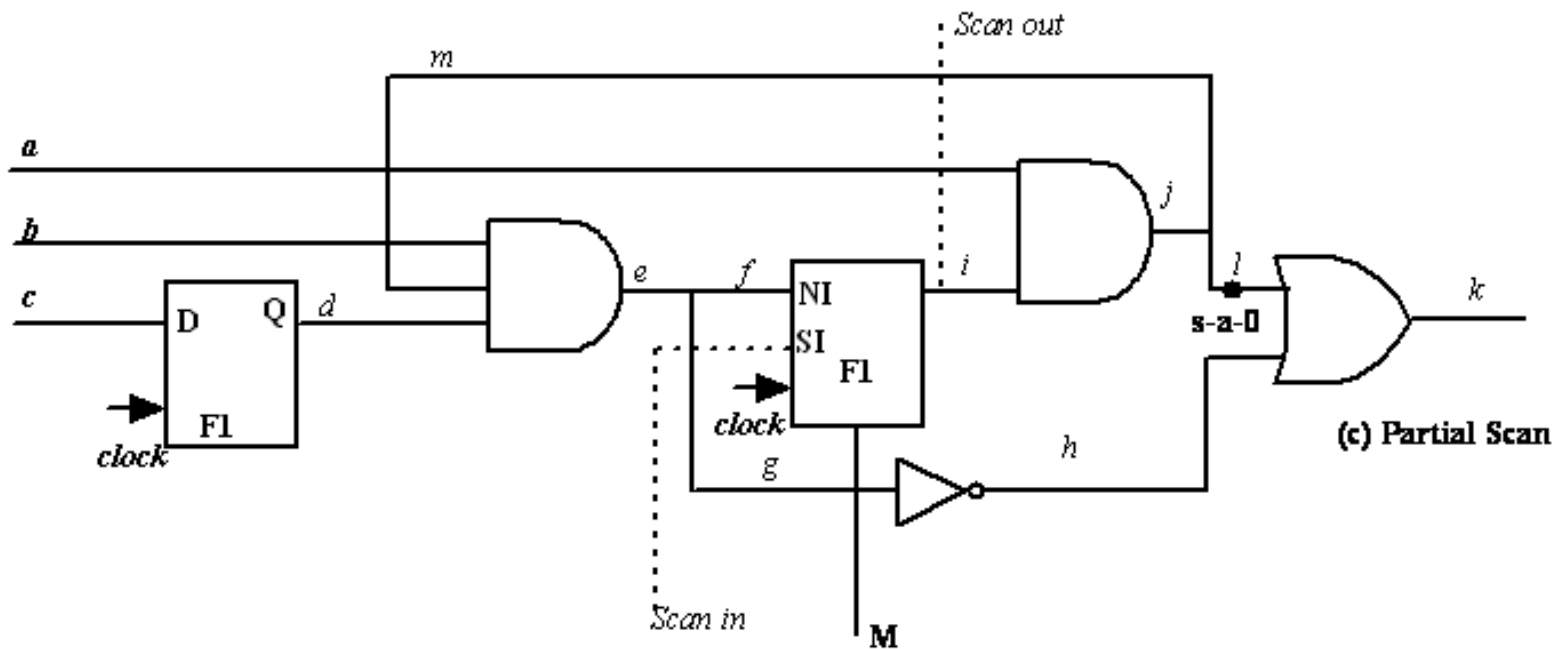
ATPG and testing using partial scan chain in a sequential circuit: An Example

- Two flip-flops are to be controlled to 1; net d is to be made 1 and net i is to be made 1. Making net $d=1$ is simple and can be achieved by applying $c=1$ and a clock pulse.
- Control of net d via F1 is by time frame expansion method; as $d_{seq}=1$ for F1, so one clock pulse and one pattern is enough to control it.

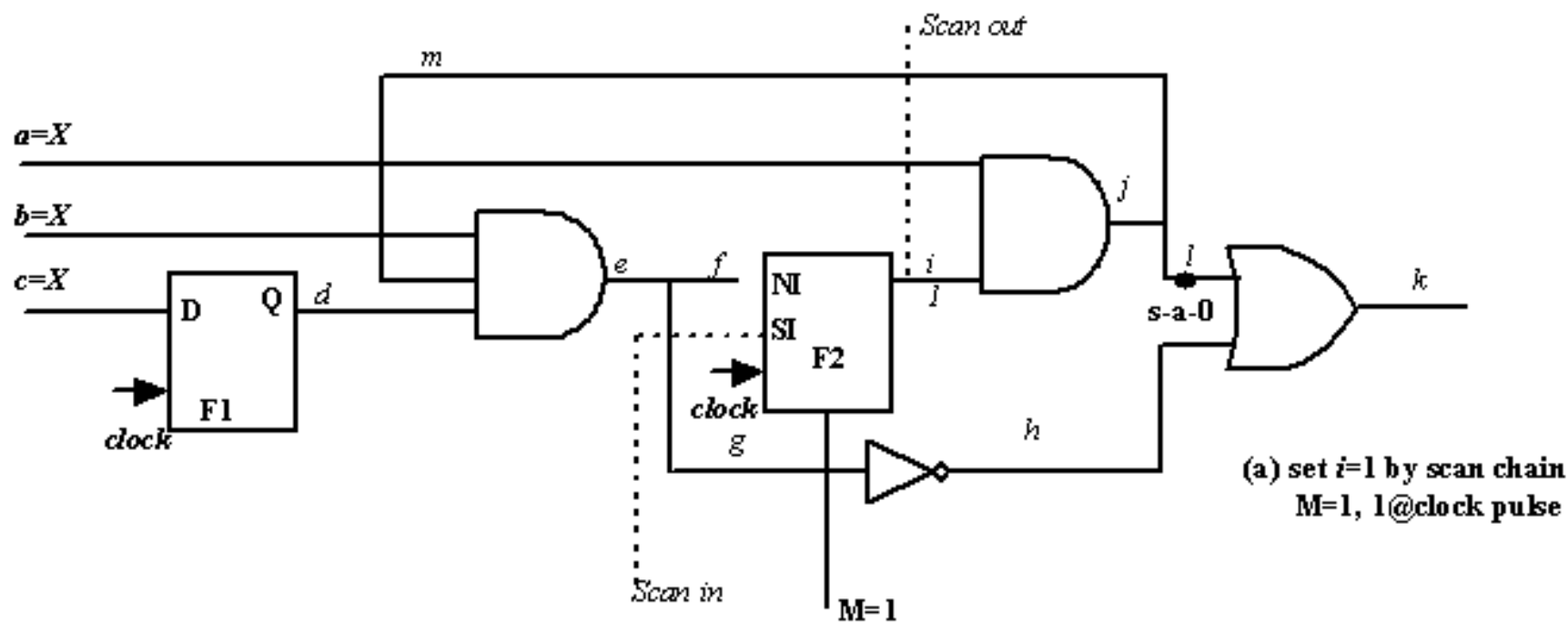


ATPG and testing using partial scan chain in a sequential circuit: An Example

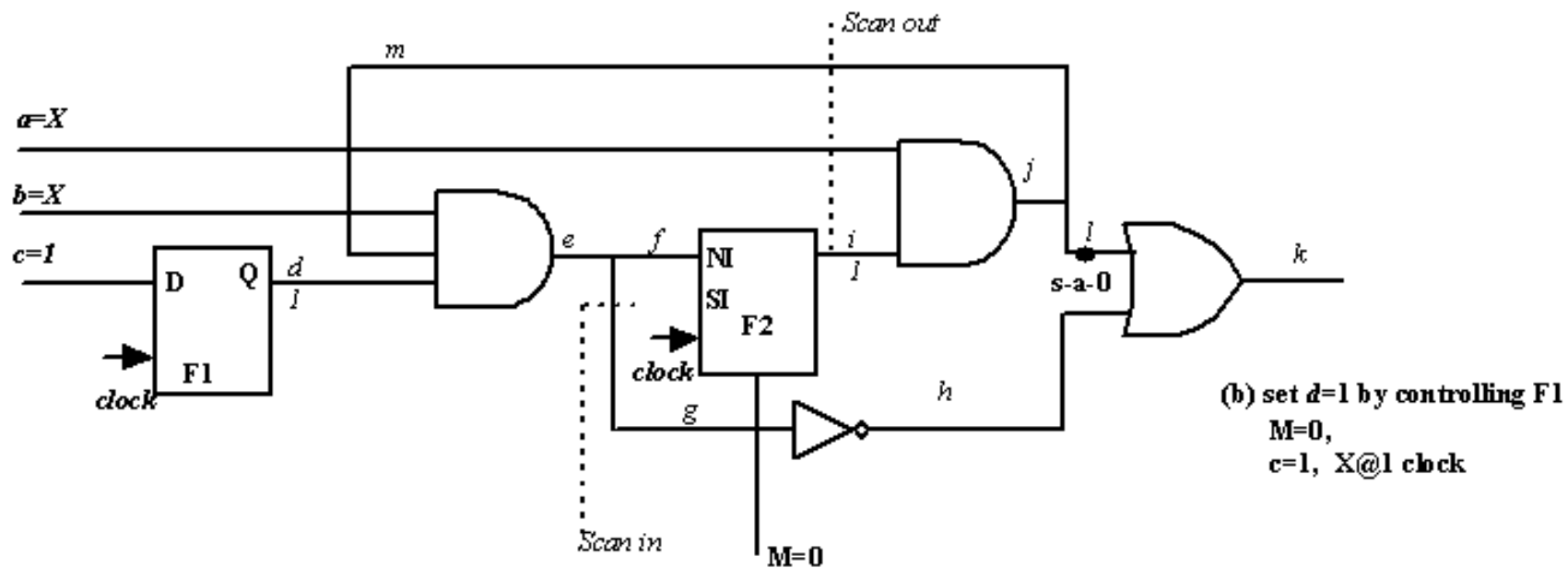
- To make net $i=1$, we need $b=1, d=1, m=1$ (which makes $f=1$ via net e) and a clock pulse.
- However there is a problem here. To make net $m=1$ we need $j=1$ which can be achieved by $a=1, i=1$. However to make $i=1$ we need $m=1$. This problem arises because flip-flop F2 is cyclic
- So F2 cannot be controlled by time frame expansion method and it must have scan chain facility.



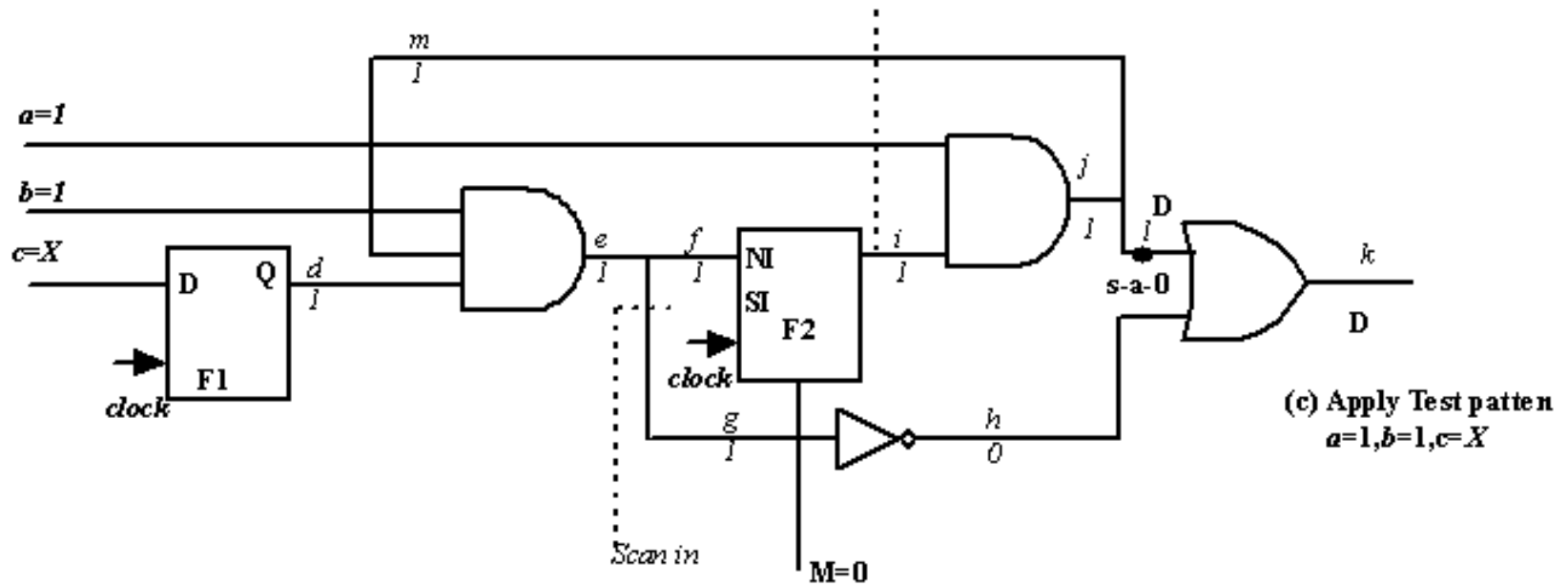
ATPG and testing using partial scan chain in a sequential circuit: An Example



ATPG and testing using partial scan chain in a sequential circuit: An Example



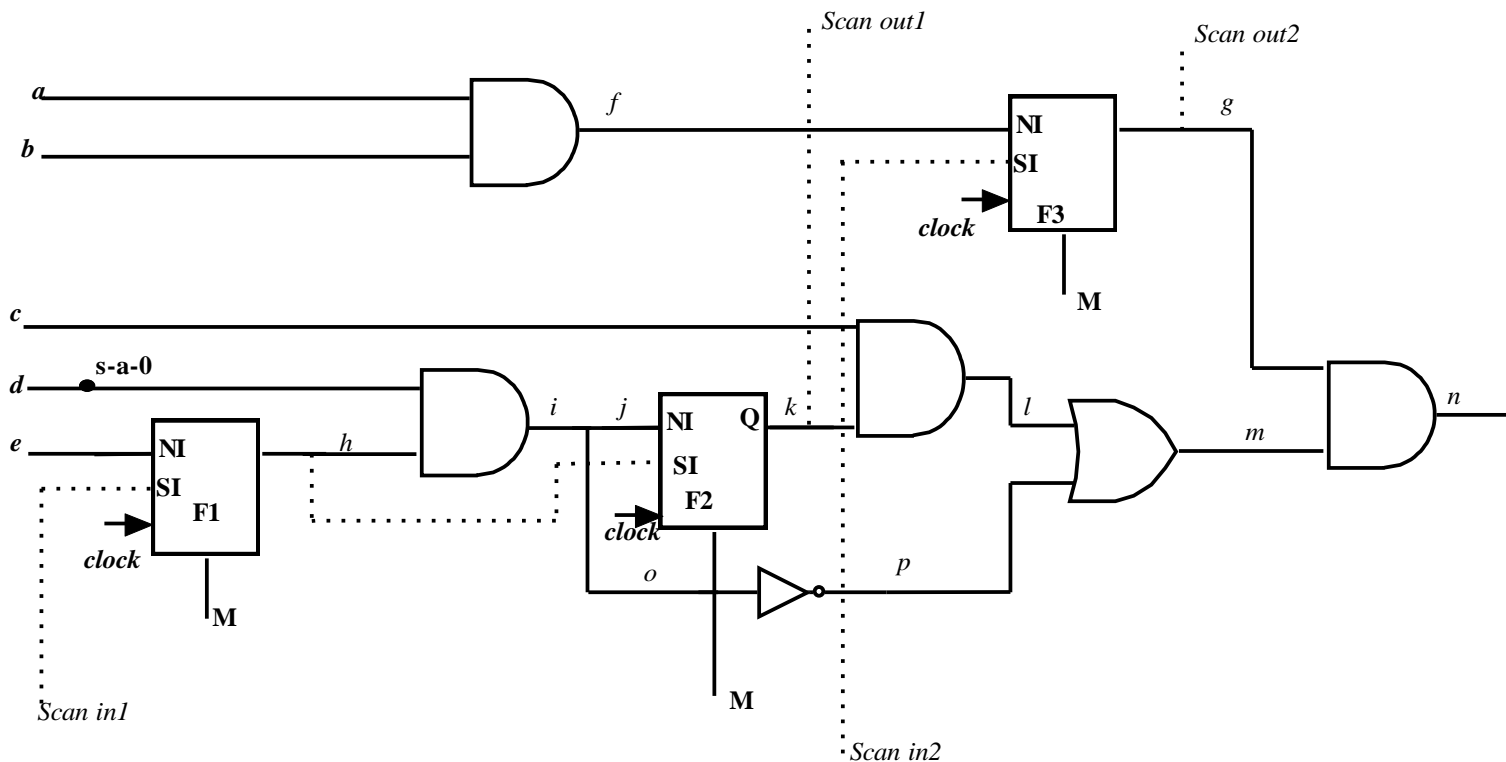
ATPG and testing using partial scan chain in a sequential circuit: An Example



Questions and Answers

Question: How can test time be reduced for the circuit below with scan chain ?

Answer: The circuit has a single scan chain with three flip-flops. So time taken to set/reset all the flip-flops is three clock pulses. To save test time the scan chain can be divided into multiple sub-chains with separate Scan in and Scan out pins. In this case we have divided the chain into 2 parts—one has F1 and F2 and the second has F3 only. So we have two sets of Scan in and Scan out pins. The design is illustrated in the figure below. Now both the chains can be loaded concurrently. So, only two clock pulses are required to set/reset all the flip-flops.



Questions and Answers

Question: How can the flip-flops themselves be tested in a scan chain based testing?

Answer:

An advantage of scan chain based testing over time frame expansion and shift register technique is the ability to test the flip-flops in the circuit under test. A toggle sequence, 00110011 . . ., of length $n_{ff} + 4$, where n_{ff} is the total number of flip-flops, is applied at Scan in. This sequence produces all four transitions $0 \rightarrow 0$, $0 \rightarrow 1$, $1 \rightarrow 0$ and $1 \rightarrow 1$ in all the flip-flops. The sequence is brought out through the Scan out pin. So if a correct toggle sequence is observed in the Scan out pin, then the flip-flops are working normally. It is shown in stuck at fault model that toggle sequence covers almost all stuck at faults in the flip-flops.

Thank You